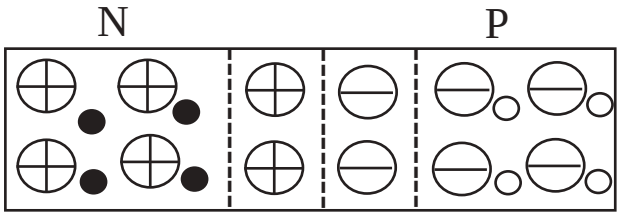
ANALOG ELECTRONICS

JUNCTION THEORY



* PN Junction is formed on a single crystal of Semiconductor like Ge or Si by dropping acceptor impurity on one side and donor impurity on the other side.
* Since P-side is having large hole as compared to electron and N-side is having large electron as compared to hole so due to difference in concentration, diffusion takes place, i.e., hole diffuse to N-side and electron diffuse to P-side.
* Depletion region is completely free from any mobile charge. It is behave just like Capacitor, which is controlled by appled voltage at P and N side.
* Forward bias causes Depletion region to shrink, so increase the value of capacitor.
* Total Depletion region width $W = W_n + W_p$
* $N_D W_n = N_A W_P$ means for highly dropped region the Depletion region is less in that side.
* Barrier Potential or Build in Potential.

$$V_B = V_T \ln\left(\frac{N_A . N_D}{n^2}\right) = \frac{KT}{q} \ln\left(\frac{N_A . N_D}{n^2}\right)$$

* Current flow in PN junction diode $= I_0\left(e^{\frac{nv}{V_T}} - 1\right)$

Where I_0 = reverse saturation current
n = Factor due to charge generation and recombination.
n = 1 for Ge. = 2 for Si

* I_0 doubles for every 10°C rise in temp.

$$I_o' = I_o \; 2^{[(T' - T)/10]}$$

* Diode dynamic resistant

$$r = \frac{dV}{dI} = \frac{1}{dI/dV} = 1/\text{Slop of characteristic of diode}$$

$$= \frac{nV_T}{I} = \frac{26(mV)}{I(mA)} \quad ; \; n = 1$$

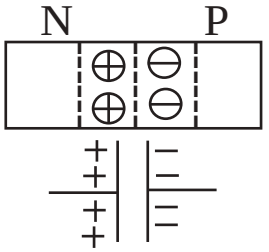
* $$I_o = q\left(n_p \frac{L_n}{\tau_n} + p_N \frac{L_p}{\tau_p}\right)$$

Where, L_n and $L_p \rightarrow$ Diffusion length

τ_n and $\tau_p \rightarrow$ Life time.

CAPACITANCE IN PN JUNCTION DIODE

The depletion region denotes a parallel plate capacitor since the total charge on the 2 side of the depletion region is equal but opposite.



$$C = \frac{\varepsilon A}{d} = \frac{\varepsilon A}{w}$$

Where, ε = permittivity of medium

A = cross section area

d = W = Total width of depletion region.

$= W_N + W_p$

Capacitance are of two type

TRANSITION CAPACITANCE

C_T arises due to reverse bias applied and due to majority charge carrier.

$$C_T(V_r) = \frac{C(o)}{1 + [V_r / V_T]^n}$$

V_r = Reverse bias voltage; C(o) = Capacitance at zero bias;

n = [1/2] for step graded/Abrupt junction

= [1/3] for diffused/linearly graded junction.

Finally, $C_T = K_1[V]^{-1/2}$: for abrupt junction

$= K_2 V^{-1/3}$: for linearly graded function

$W_B = K_1[V_j]^{1/2}$: for abrupt junction

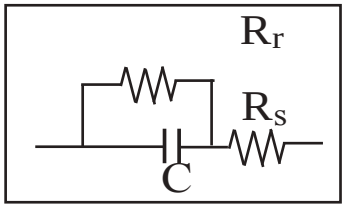
$= K_2[V_j]^{1/3}$: for linearly graded junction.

Diffusion Capacitance C_D exist for forward bias and is important for minority charge carrier

$$C_D = \frac{\tau_n}{r_n} + \frac{\tau_n}{r_p}$$

Where, τ = Life time;
r = Dynamic resistance of region

* Diffusion Capacitance increase rapidly with forward bias i.e. $C_D \propto I$.
* The value of C_D is of the order of several þF and hence it is important when high frequency circuit for transistor are derived.
* Voltage variable diode capacitor are called Varactor, Varicap or Volta cap. They are used in frequency modulation circuit.



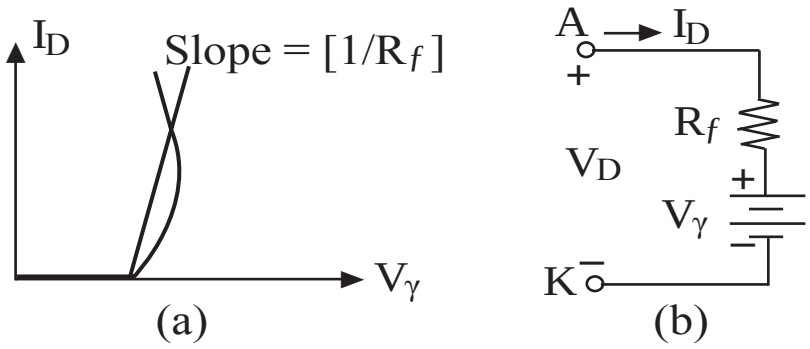
* $L = \sqrt{D\,\tau}$

Where L = Diffusion length, D = Diffusion Coefficient
τ = Life time

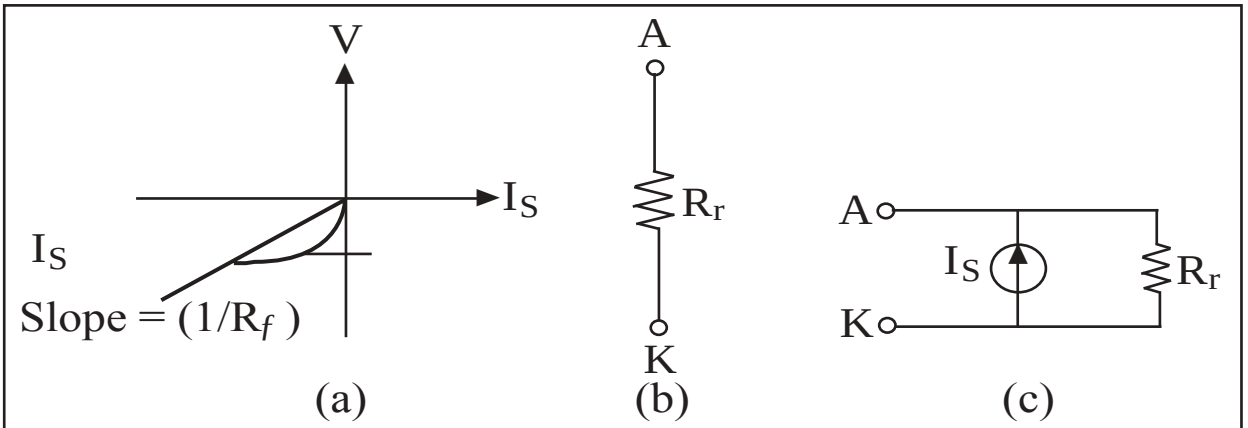
The Einstein relation $\dfrac{D}{\mu} = V_T = \dfrac{KT}{q}$

DIFFERENT TYPES OF DIODES AND THEIR CHARACTERISTIC

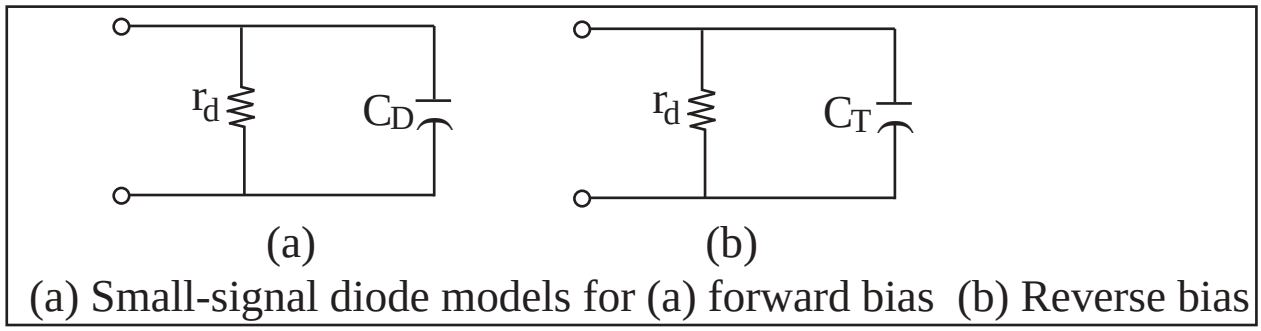
DIODE



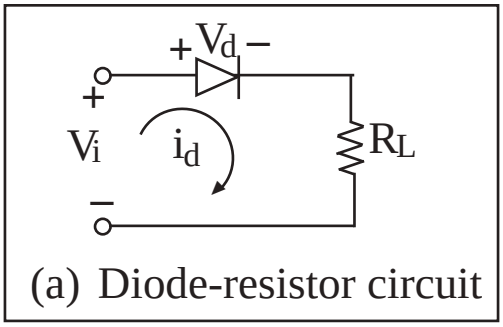
(a) Piecewise linear diode forward characteristic
(b) Diode model for forward bias.



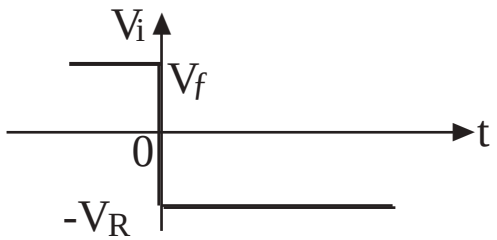
(a) Piecewise linear reverse characteristic of diode
(b) Diode model based on piecewise linear representation.
(c) Model to include surface leakage



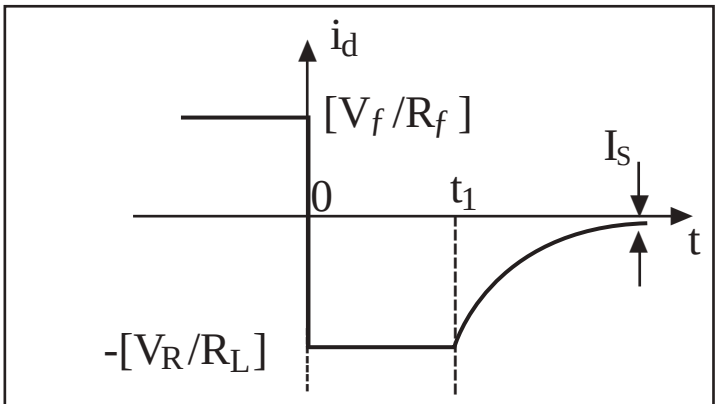
(a) Small-signal diode models for (a) forward bias (b) Reverse bias



(a) Diode-resistor circuit

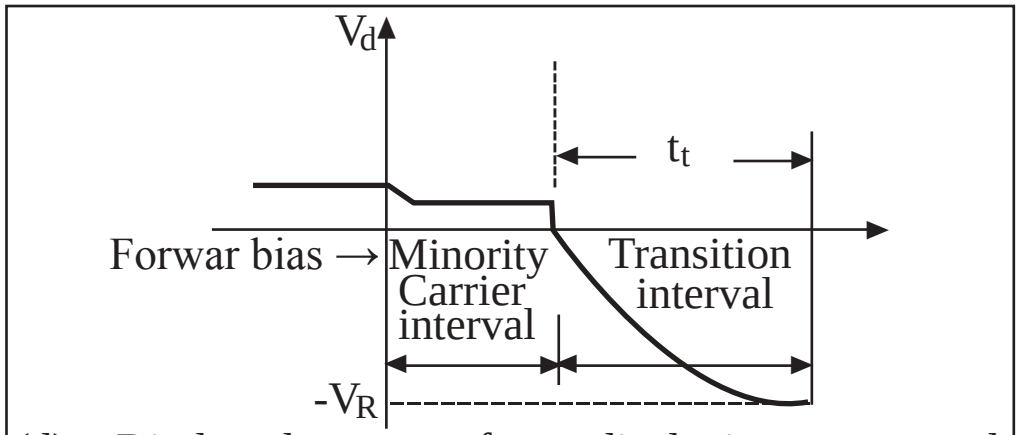


(b) Input waveform applied to circuit in part figure (a) Showing abrupt change from forward to reverse bias.



(c)

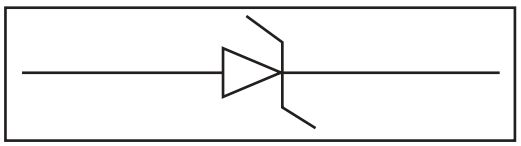
(c) Diode current



(d) Diode voltage waveforms displaying storage and transition times.

ZENER DIODE

It is a PN junction diode with heavy doping Operate under reverse bias condition and for voltage > V_g .
(Breakdown voltage)



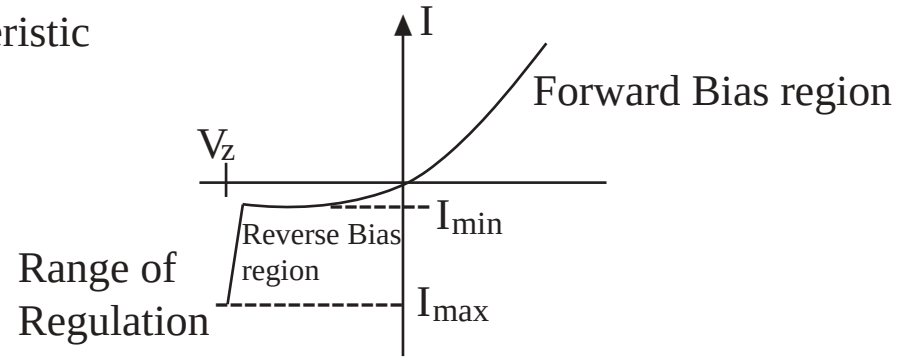
BREAKDOWN MECHANISM

Zener breakdown and Avalanche breakdown

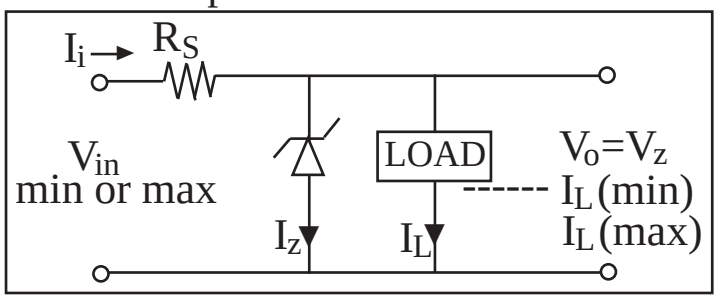
Zener Breakdown

1. This phenomenon occur in PN junction diode with very high doping.
2. It occur when the diode is reverse bias of voltage approximately 4 to 6 V.
3. The junction is narrow since the width of depletion layer is small become of highest doping and relatively low reverse bias voltage.
4. The junction width is of the order of 100Aº so that very strong electric field of 10^7 V/m is developed near the junction
5. Now as the reverse bias voltage is increased then the current will be only due to minority charge and is of the order is μA or nA.
6. As the reverse voltage is still increased a value of this voltage is reached so that very high electrical field is developed.
7. For this magnitude of the electrical field there will be direct rupture of the covalent bond so that immediately a number of free charge carrier is generated.
8. At this voltage we say that the zener breakdown has occur and because of increase number of free charge carrier conductivity of the region increases.
   Therefore, the current suddenly increasing maintaining a constant potential across the PN junction. This constant voltage is called the zener breakdown voltage.
9. $V < V_z$; $I \cong 0$
   $V \geq V_z$; $I =$ Suddenly increase
10. $V < V_z$ The dynamic resistance is very large
    $V \geq V_z$ The dynamic resistance is small.

11. Characteristic



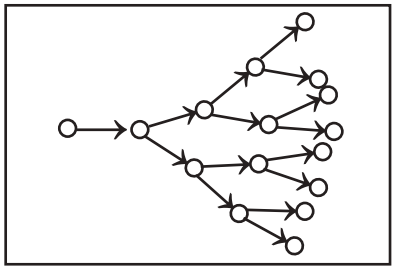
12. In the forward bias condition the V - I characteristic is of the similar nature of ordinary diode.
13. The V - I characteristic of forward bias condition is not practically useful since the same variation we can get using an ordinary PN junction diode.
14. The increase in the current, once the breakdown has occur is limited by the use of a series of resistor along with the zener diode the current varies from I_{min} to I_{max}. I_{max} = I (rated current)
15. Practically for designing a circuit, we use I_{min} to the 20% of 1 (rated). $I_{min} \cong$ 0.2 I rated I_{max} = 0.8 I(rated)
16. This device can be utilized as a voltage regulator since the voltage across it remain constant irrespective of current variation through it.

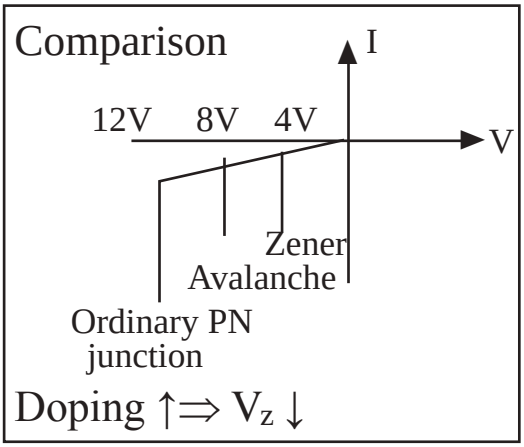


Avalanche Breakdown

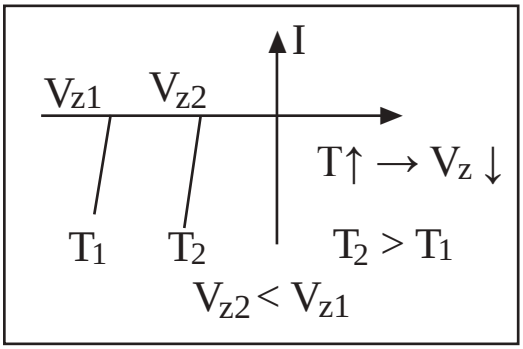
1. This breakdown occurs in PN junction diode with reverse bias applied.
2. The doping in much greater than that used in the ordinary PN junction diode but is smaller than that of a diode in which zener breakdown occur, i.e. $D_{zener} > D\text{-}_{avalanche} > D\text{-}_{ordinary}$
3. The reverse bias voltage applied relatively higher of the order of 8 to 10 V depending upon doping.
4. The width of depletion layer is relatively more than that in the diode with zener breakdown.

5. Since the reverse bias voltage applied is relatively large an free charge carrier say electron acquire high K.E and strike an atom. The covalent bond is broken and other free-electron is librated so that now there are two free electron available for conduction.
6. Since the applied voltage is maintained high there two electrons again acquire high K.E., striking other atom and librating two more free electron ad so on.
7. At a given voltage called the avalanche breakdown voltage a number of free charge carrier are available to avalanche multiplication as shown so that the conductivity of the region suddenly increase. Therefore the current suddenly increase maintaining a constant potential to the junction.





Variation V_z with temperature

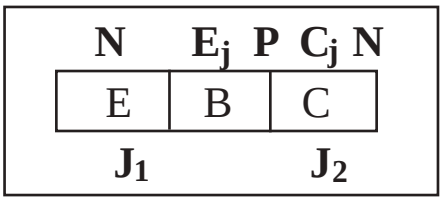


Dynamic Resistance $r = \frac{\Delta V}{\Delta I}$

= Very large for $V < V_z$
= Very small for $V > V_z$

8. The VI characteristic is similar to that a diode with zener breakdown.

CHARACTERISTICS OF BJT
BJT: BIPOLAR JUNCTION TRANSISTOR



Collector region width is maximum
(a) To collect maximum number of charge carrier.

(b) To reduce heat dissipation (per unit area surface).

Depletion layer in collector junction base side is maximum Emitter junction. Emitter side is Minimum.

Biasing and application

Input Jn J_1 (EB J_n)	Output Jn J_2 (CB J_n)	Region in which BJT works	Application
FB	RB	Active	Amplifier
FB	FB	Saturation	BJT is ON or OFF
RB	RB	Cut off	OFF
RB	FB	Invented (Active)	Amplifier with decreased gain α_1 , β_1

* For Normal Biasing (i.e. Emitter junction FB and Collector junction RB) the emitter junction has low resistance.

EARLY EFFECT

For active region operation of transistor collector base region is reversed biased. Due to reverse bias the depletion width in base region increases which causes effective width of base to decrease. This effect is known as early effect.

If the reverse bias VcB is increased beyond a point, breakdown may occur as width of base becomes zero and phenomena is called punch through or Base width modulation.

THE PHYSICAL BEHAVIOR OF BIPOLAR TRANSISTOR

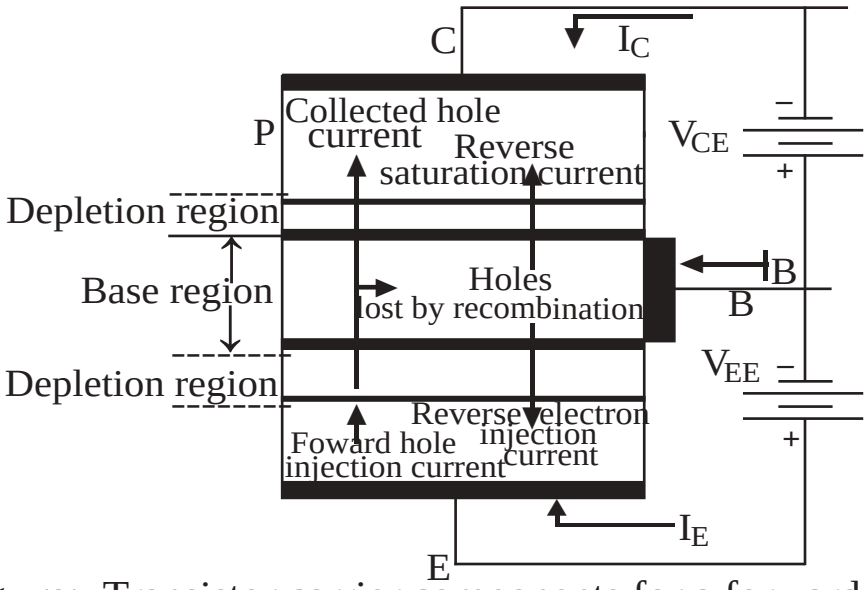


Figure: Transistor carrier components for a forward biased emitter-base junction and reverse biased collector base junction.

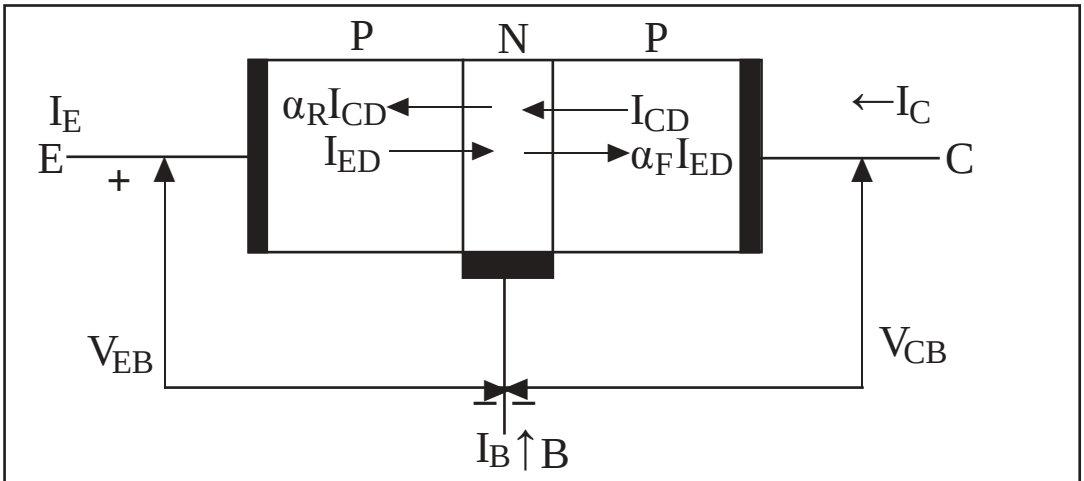


Figure: Current components in PNP transistor

On the basis of the considerations in the preceding paragraph we construct the Ebers-Moll mode in below figure. The two back to back diode (whose cathodes are connected) represent the junctions of the bipolar transistor, whereas the two controlled sources indicate the coupling between junctions.

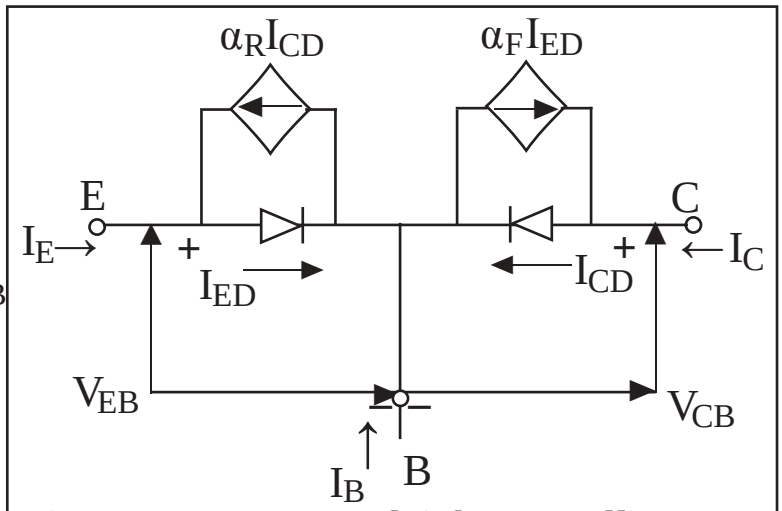


Figure: Large-signal (Ebers-Moll) representation of a PNP transistor.

The current I_{ED} and I_{CD} are related to V_{EB} and V_{CB} by the diode volt ampere relation given in the equation. Thus the I_E and I_C can be expressed in terms of the two diodes currens as

$$I_E = I_{ED} - \alpha_R I_{CD} = I_{ES}\left[\left(e^{V_{EB}/V_T}\right) - 1\right] - \alpha_R I_{CS}\left(e^{V_{CB}/V_T}\right)$$

$$I_C = -\alpha_R I_{ED} + I_{CD} = -\alpha_F I_{ES}\left(e^{V_{EB}/V_T} - 1\right) + I_{CS}\left(e^{V_{CB}/V_T} - 1\right)$$

The relationship expressed in above two equations are known as the Ebers-Moll equations.

The quantities I_{ES} and I_{CS} in above equation are reverse saturation currents of emitter ase and collector base junction, respectively. The parameter α_F and α_R are each less than unity as not all the current from

one diode is couple to the other junction. The subscript refer to forward (F) transmission from emittor to collector and reverse (R) transmission from collector to emitter.

$$\alpha_F I_{ES} = \alpha_R I_{CS} \quad \text{and} \quad I_B = -(I_E + I_C)$$

$$I_E = -I_{ES}\left[e^{\left(\frac{V_{EB}}{V_T}\right)} - 1\right] + \alpha_R I_{CS}\left[e^{\left(\frac{V_{CB}}{V_T}\right)} - 1\right]$$

$$I_C = \alpha_F I_{ES}\left[e^{\left(\frac{V_{EB}}{V_T}\right)} - 1\right] - I_{CS}\left[e^{\left(\frac{V_{CB}}{V_T}\right)} - 1\right]$$

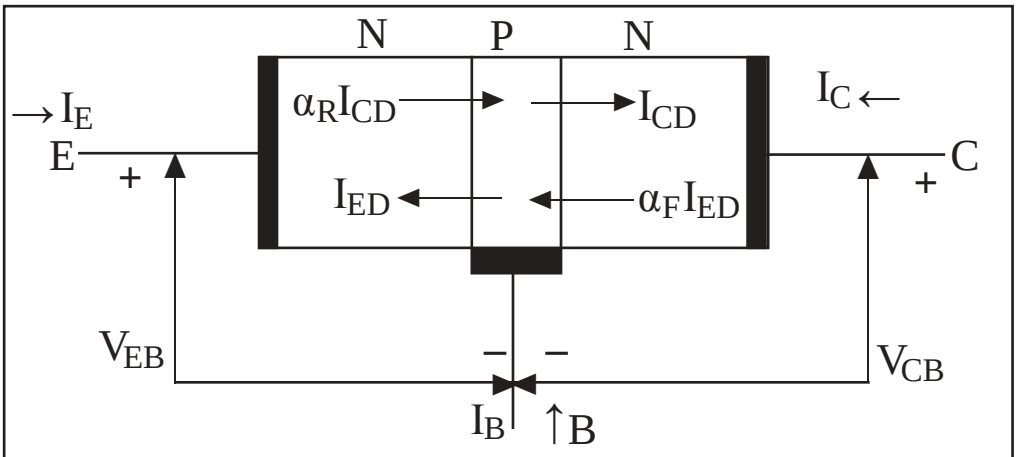


Figure: Current component in NPN transistor

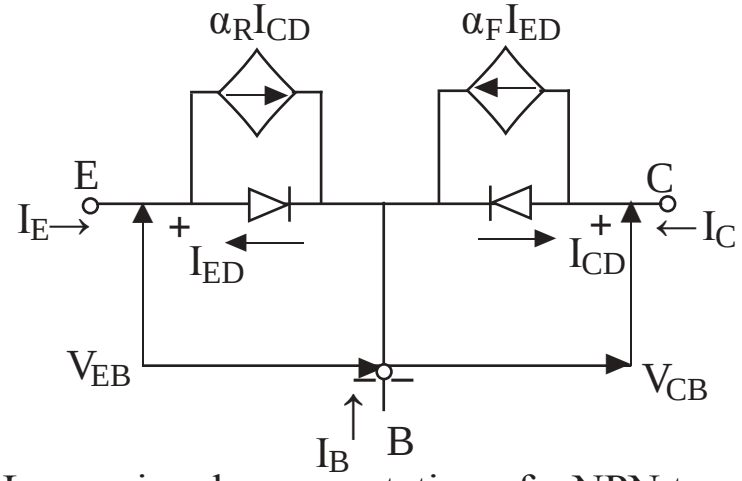


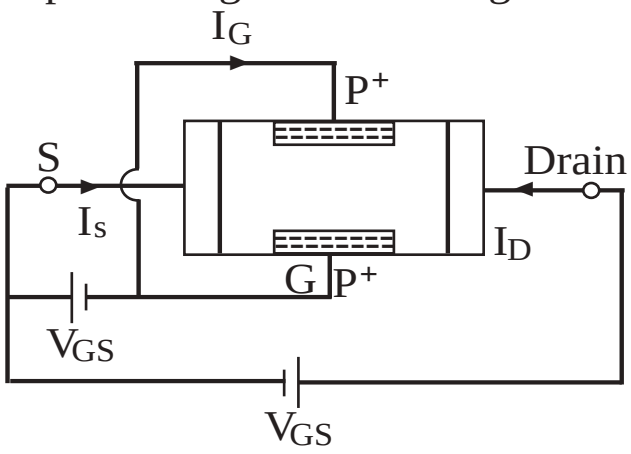
Figure: Large-signal representation of a NPN transistor

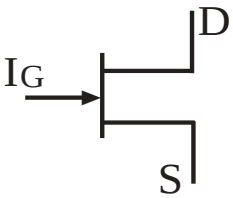
CHARACTERISTICS OF JFET

TWO TYPES: N CHANNEL AND P CHANNEL

It consists of a semiconductor block which is n type for n channel and p type for p channel. On both sides of n block acceptor impurities p are heavily doped by allowing or by diffusion. The region is called the gate. Ohmic contact are attached to the either ends of the n-block. One end is called Source and other is called Drain. The np region between source

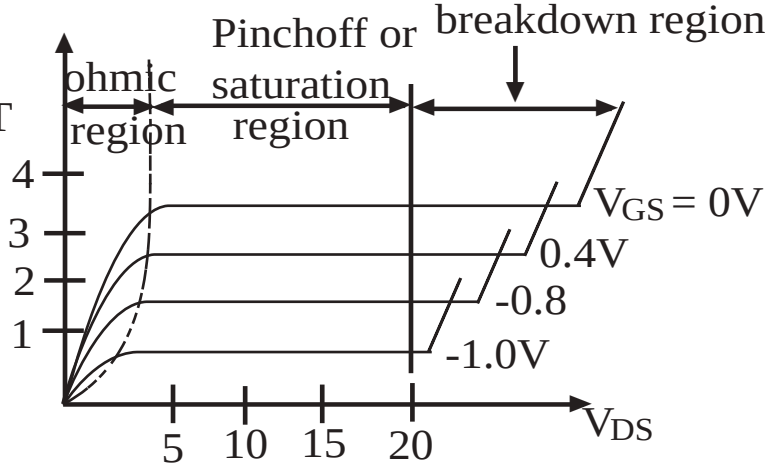
and gate is reverse biased. In the vicinity of np junction there is diffusion of majority carriers, electrons and holes leaving uncover immobile positive and negative ions. When RB is applied, the space charge width increases uncovering more ions, until the space charge region from the two end, meets the n type region between the two (P^+) gates is called n channel and when a positive voltage is applied between drain and source, there is a current flow in the channel of majority carriers, (electrons). When a reverse bias is applied between the gate and source, constriction of the channel takes place by widening of the space charge depletion region controlling the flow of electrons to the drain.





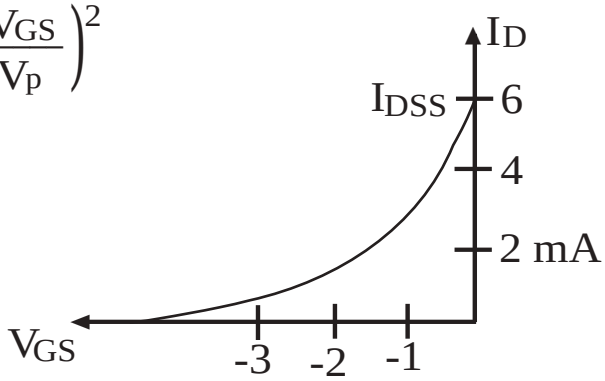
Symbol of n-channel FET

Note : For a P channel FET the bar is a P type semiconductor and gate is dopped by n^+ donor impurity.



N-Channel FET characteristic

$$I_{DS} = I_{DSS}\left(I - \frac{V_{GS}}{V_p}\right)^2$$



FET Transfer characteristic

1. Drain resistance $r_d = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS} = \text{Constant}}$

Output resistance of FET and evaluated in constant drain current region of V_{DS} - I_D curve. It is of the order of 10 to 20 kΩs.

2. Transconductance $g_m = \left.\frac{I_D}{V_{GS}}\right|_{V_{DS} = \text{Constant}}$

It will be of the order of 2 k to 6 k micromhos.

3. Amplification Factor $\mu = g_m r_d$

4. $= \frac{V_{DS}}{I_D} \times \frac{I_D}{V_{GS}} = \frac{V_{DS}}{V_{GS}}$, It ranges of 40 to 100.

5. Input resistance $r_{GS} = \frac{V_{GS}}{I_{GSS}}$

It is of the order of hundruds of megaohmes. FET is high impedance device.

VARIOUS RELATIONSHIP OF FET

Pinch off voltage $V_p = \frac{eN_D a^2}{2\varepsilon}$

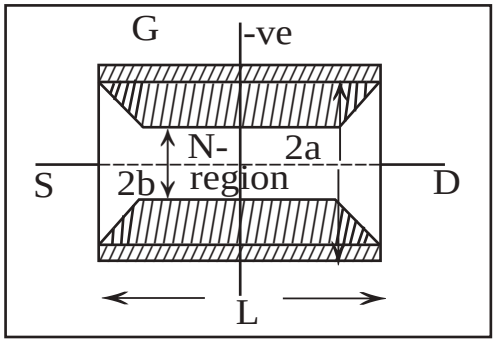
2a → Width of channel without any gates bias.
2b → Width of channel after bias.
L → Length of the channel.

$b = a\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]$; when $V_{GS} = 0$, $b = a$

If w → channel dimension perpendicular to b direction.

$A = 2bW$

Drain Current $I_D = AqN_D \mu_n E = 2bwq\, N_D \mu_n \frac{V_{DS}}{L}$



Substituting 'b' $I_D = \frac{2awqN_D\mu_n}{L}\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right] V_{DS}$

The ON resistance $r_d = \frac{V_{ds}}{I_d}$ $\quad r_{dON} = \frac{L}{2awqN_D\mu_n}$ for $V_{GS} = 0$

Transfer Characteristics

In amplifier application, the FET is almost used in the region beyond pinch-off (also called the constant-saturation region).

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Relation between g_m, I_{DDS} and I_{DS}

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad ....(1)$$

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS}\,2\left(1 - \frac{V_{GS}}{V_p}\right)\left(\frac{-1}{V_p}\right)$$

$$g_m = \left(\frac{-2I_{DDS}}{V_p}\right)\left(1 - \frac{V_{GS}}{V_p}\right) \quad ...(2)$$

g_{mo} = It is value of g_m for $V_{GS} = 0$ and given by $g_{mo} = \left(\frac{-2I_{DSS}}{V_p}\right)$ ...(3)

now $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$ ...(4)

From equation (1) $\left(1 - \frac{V_{GS}}{V_p}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$ ...(5)

From equations (2) and (5)

From the transfer characteristic we have

$$g_m = \frac{-2I_{DSS}}{V_p}\sqrt{\frac{I_{DS}}{I_{DSS}}} = \frac{-2}{V_p}\sqrt{I_{DS}\cdot I_{DSS}} \qquad |g_m| = \frac{2}{|V_p|}\sqrt{I_{DS}\cdot I_{DSS}}$$

CHARACTERISTICS OF MOSFET

DEPLETION TYPE MOSFET

The real name of MOSFET is IG FET, i.e., insulated gate field effect transistor. The gate insulated from the substrate by an oxide layer.

In the FET the metal and channel with dielectric in between forms a parallel plate capacitor giving rise to a high input impedance of (10^{10}) to (10^{15}) ohms and is the major difference from JFET. There are two types of MOSFET enhancement and depletion type.

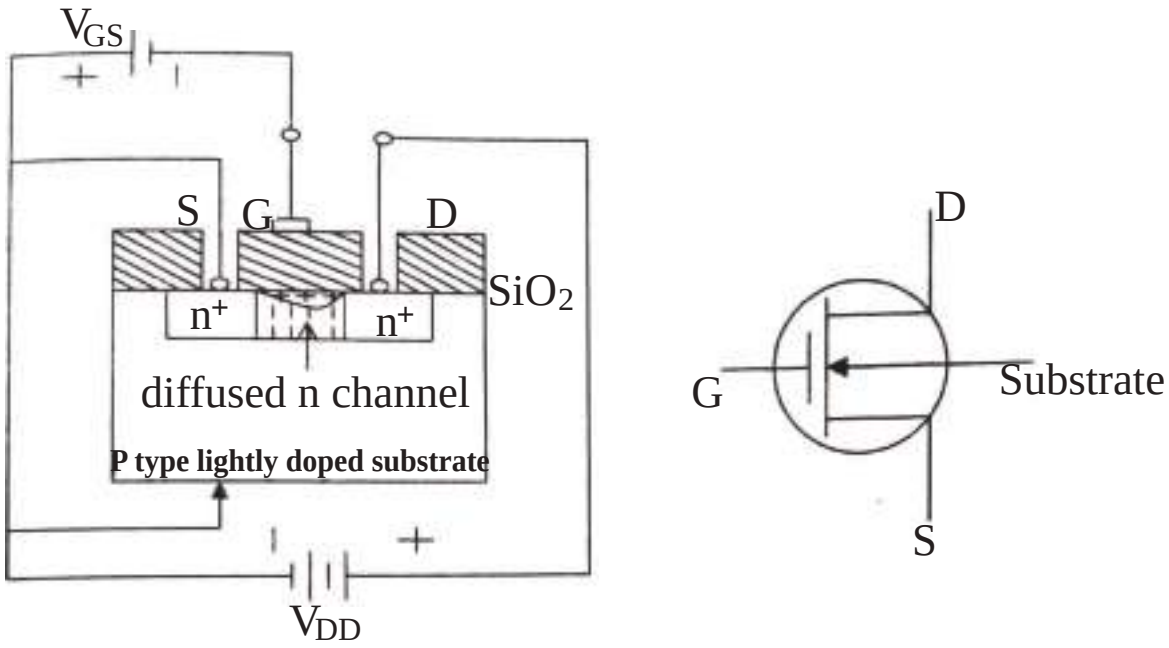
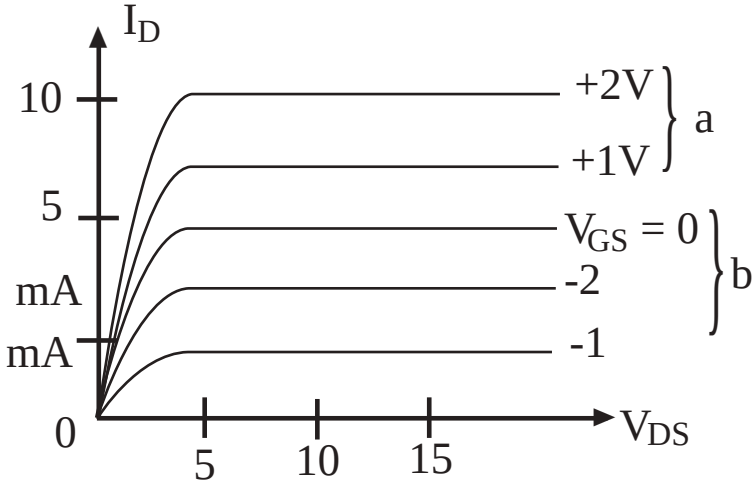
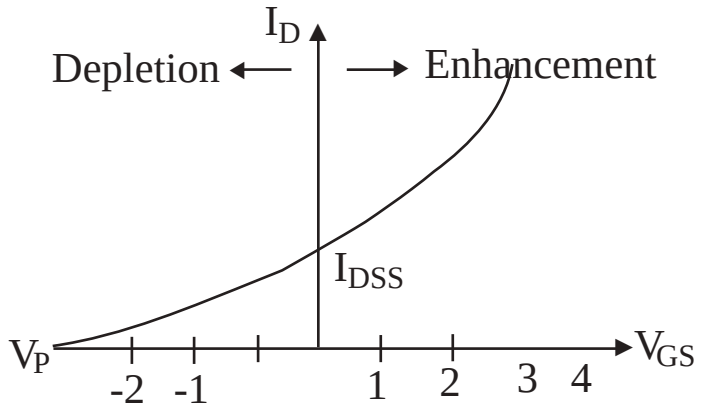


Figure: Symbol of n channel depletion type MOSFET

When a negative voltage V_{GS} is applied to the conducting terminal of the capacitor positive charges are induced in the channel, the other side of the capacitor. These positive charge neutralize the electrons in the n channel and reduce the charge carrier. This reduces the drain current. The depletion region is wider as in JFET near the drain than the near the source, due to voltage drop by the drain current. Unlike JFET when gates is reverse biased, MOSFET there is no pn^+ junction. As the carrier, electron, in n channel are depleted this is called depletion type MOSFET.
The same MOSFET can be made enhancement type when a positive voltage is applied to the gate negative charge are induced in the channel adding to the electron, charge carrier in the channel this enhances the drain current.



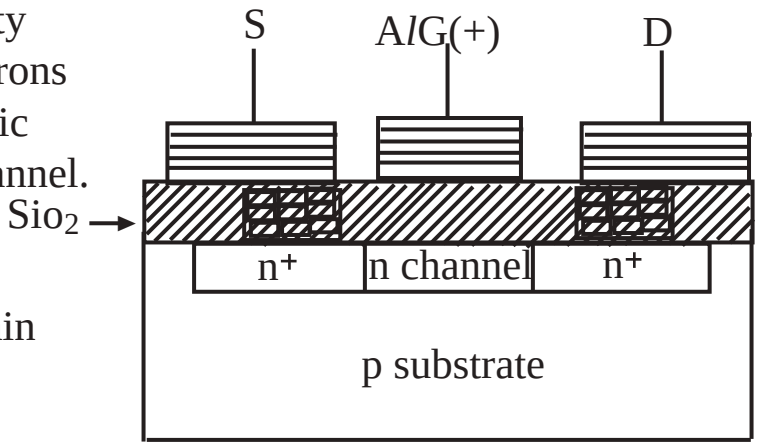
Depletion MOSFET Characteristic



Depletion N-MOSFET Transfer Characteristic

ENHANCEMENT TYPE MOSFET

No channel is diffused in the P substrate. So when a positive voltage is applied to the gate, the minority carries is the P substrate, electrons are drawn towards the dielectric and this forms an effective channel. As the positive voltage on the gate is increased, conductivity increases leading to higher drain current as the negative charge carrier are increased.



(Positive Gate voltage greater than V_T is applied)

Figure : Enhancement in n-channel MOSFET

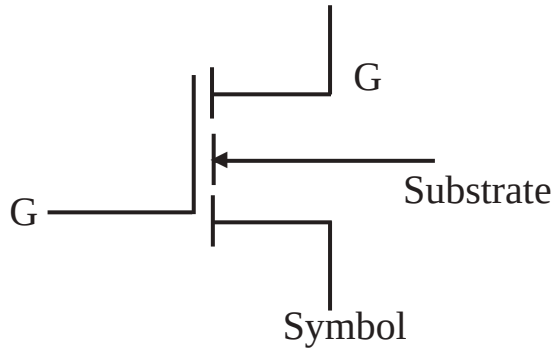
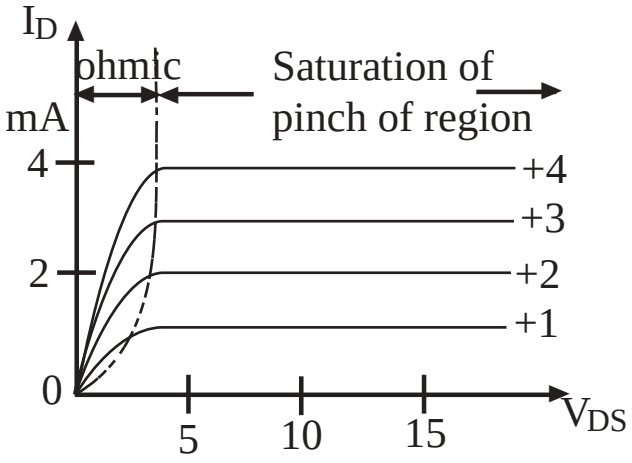


Figure : Symbol of n-channel enhancement MOSFET



Enhancement N-MOSFET Characteristics

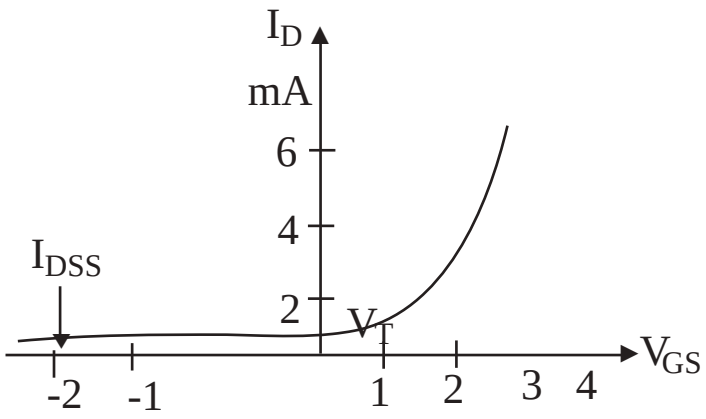


Figure : Transfer characteristic of N-channel E-MOSFET

* We note from the transfer characteristics that a threshold voltage V_{GST} is required for drain current to flow. Without gate voltage, a small current of nanoampere I_D flows in the drain.
* The electric field produced by the gate voltage is largest near the source and least near the drain.
* For pinch of $V_{PDS} = V_{GS} - V_T$

Compassion between FET ad SMOSFET

1. A current-controlled device is one in which a current defines the operating conditions of the device, whereas a voltage-controlled device is one in which a particular voltage defines the operating conditions.
2. The JFET can actually be used as a voltage controlled resistor because of a unique sensitivity of a the drain-to-source impedance to the gate-to-source voltage.
3. The maximum current for any JFET is labeled I_{DSS} and occurs when $V_{GS} = 0$ V.
4. The minimum current for a JFET occurs at pinch-off defined by $V_{GS} = V_P$.
5. The relationship between the drain current and the gate to source voltage of a JFET is a nonlinear one defined by Shockley's equation. As the current level approaches I_{DSS} the sensitive of I_D to changes in V_{GS} increases significantly.
6. The transfer characteristics (I_D versus V_{GS}) are characteristics of the device itself and are not sensitive to the network in which the JFET is employed.

7. When $V_{GS} = V_P/2$, $I_D = I_{DSS}/4$; and a point where $I_D = I_{DSS}/2$, $V_{GS} = 0.3$ V.
8. Maximum operating conditions are determined by the product of the drain-to-source voltage and the drain current.
9. MOSFETs are available in one of two types : depletion and enhancement.
10. The depletion-type MOSFETs has the same transfer characteristics as a JFET for drain currents up to the I_{DSS} level. At this point the characterstics of a depletion point type MOSOFET continue to levels above I_{DSS} . Whereas those of the JFET will end.
11. The arrow in the symbol of n-channel JFETs or MOSFETs will always point in to the center of the symbol, whereas those of a p-channel device will always point out of the center of the symbol.
12. The transfer characteristics of an enhancement-type MOSFET are not defined by Shockly's equation but rather by a nonlinear equation controlled by the gate to source voltage, the threshold voltage, and a constant k defined by the device employed. The resulting plot of I_D versus V_{GS} is one that rises exponentially with increasing values of V_{GS}.
13. Always handle MOSFETs with additional care due to the static electricity that exists in places we might least suspect. Do not remove any shorting mechanism between. The device until it is installed.
14. A CMOS (complementary MOSFET) device is one that employs a unique combination of a p-channel an n-channel MOSFT with a single set of external leads. It has the advantages of a very high input impedance, fast switching speeds, and low operating power levels, all of which make very useful in logic circuits.

JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad I_D = I_{DSS}\,{}_{V_{GS} = 0V}\ ;\ I_D = 0\ \text{mA}\Big|_{V_{GS} = V_P}$$

$$I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2} \qquad V_{GS} = 0.3\ V_P\Big|_{I_o\ = I_{DSS/2}}\ ;\ V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS}\, I_D \qquad r_d = \frac{r_0}{(1 - V_{GS}/V_r)^2}$$

MOSFET (Enhancement) :

$$I_D = k(V_{GS} - V_T)^2 \qquad k = \frac{I_{D(on)}}{(V_{GS(on)} - V_r)^2}$$

Typical values for JFET and MOSFET

Parameter	JFET	MOSFET
Input resistance r_{gs}	$> 10^9\,\Omega$	$> 10^{13}\,\Omega$
Transconductance g_m (μ mho)	1 K to 2.5 K	1 K to 20 K
Drain resistance r_d (ohm)	0.1 M to 1 M	1 K to 50 K
Revere current I_{GSS}	0.1 to 10 nA	0.1 to 10 pA
Capacitance C(G to D)	1 to 4 pF	0.005 to 1 pF

For D-MOSFET

Characteristic are similar to FET

For E-MOSFET

$$V_{DS\ sat} = V_{GS} - V_T$$

For $V_{GS} << V_T$, the drain current of an enhancement type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship.

$$I_D = K(V_{GS} - V_T)^2$$

Where, K → constant that is function of the construction of the device, the value of K can be determined from

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

$I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristic of the device.

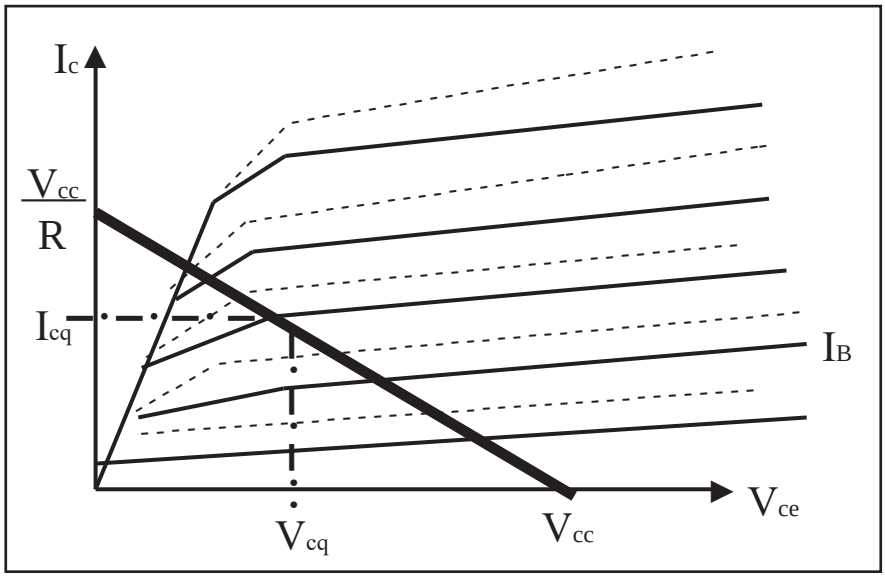
Compassion between BJT and FET

	BJT	FET
1.	High voltage gain	Low voltage gain
2.	Low current gain	High current gain
3.	Low input and output impedance	High input and output impedance
4.	Medium noise generation	Low noise generation
5.	(Gain × band-width) high	(Gain × Band-width) medium
6.	Current source	Voltage controlled

Biasing and Stabilization

The transistor is biased (with the help of external voltage in such a manner so the Q-point is selected in the middle portion the transistor output characteristic.When the ac voltage is superimposed it is ensure that the positive and negative half of input voltage cycle remain it the linear or active region if the transistor characteristic. Under these condition the transistor output voltage is undistored.

- To fix the Q-point load line curve is needed.
- The dc load line is locus of variation of output voltage and output current.
- The load lines are being drawn for the amplifier chosen in the active region of output of characteristic.
- The Q-point is generally fixed at the middle of load line.
- Ac load line have greater slope than dc load line.
- If the Q-point is chosen near the V_{ce} (Cut-off region or I_c axis (saturation region) than output will be highly distorted.
- If the Q-pont is chosen in the saturation region for NPN transistor, it may cause the output to be clipped in the positive half cycle of the input signal.



Stabilization

Once the Q-point has been fixed due to some biasing arrangement it has to be stabilized against the variation in :

(a) Temperature (T) - I_{co} double for every 10 degree rise in temperature.

(b) I_B (depends on V_{be}), i.e. V_{be} decrease at the rate of 2.5 mv/degree.

(c) β

- Due to variation of one or all of these parameter I_c current will change which shift the Q-point.
- In stabilization technique resistive biasing circuit is used which permit I_b to

vary by an amount so as to keep I_c relatively constant with variation in any of T, I_b,β

Change in Temperature

- We know that $I_c = \beta I_b + (1 + \beta) I_{co}$
- β varies due to change in temp.
- I_b also change due to change in temp. As the cut in voltage is increases at 2.5 mv/degree for constant I_c.
- I_{co} changes with temperature doubling with every 10 degree rise in temperature. Increase in I_{co} caused an increase in I_c which further increasing the collector dissipation thereby increasing the collector temperature. This may set in a cumulative effect causing thermal runway burning out the transistor ultimately.

= Si transistor, I_{co} is of the order of nano amperes compared to milliamps in Ge and so thermal runway and instability is more problem in Ge transistor.

Stability Factor

- The merit of a biasing circuit in holding the dc collector current I_c at the operating Q-point may be examine by stability factor.

$$S = \frac{\delta I_c}{\delta I_{co}} \Big|_{V_{be}}, \quad \beta = \text{constant}$$

$$S_\beta = \frac{\delta I_c}{\delta \beta} \Big|_{I_{co}} \quad V_{be} = \text{constant}$$

$$Sv = \frac{\delta I_c}{\delta V_{bo}} \Big|_{I_{co}}, \ \beta = \text{constant}$$

- Lower the value of stability factor (S) better is stability of circuit.
- $1 < S < 1 + \beta$
- The stability factor S is most important since it depends upon I_{co} and temperature.

$$S_\beta = \frac{\delta I_c}{\delta I_\infty} \Big|_{V_{be} = \text{Constant}}$$

$I_c = \beta I_b + (1 + \beta) I_{co}$ . . . generally expression

Differential with respect to I_c

$$1 = \beta \frac{\delta I_b}{\delta I_c} + (1 + \beta) \frac{\delta I_{co}}{\delta I_c}$$

$$S = \frac{\delta I_c}{\delta I_{co}} = \frac{(1 + \beta)}{(1 - \beta) \frac{\delta I_b}{\delta I_c}}$$

• For fixed bias arrangement I_b is independent of I_c,

$$S = \beta + 1$$

• Collector to base biasing :

$$S = \frac{1+\beta}{1+\frac{\beta R_c}{R_b + R_c}}$$

(a) Better than fixed biased circuit.

(b) $\beta R_c >> R_b$ as this will give very small value as stability as near to 1.

Drawback of Collector to Base Bias

• R_b has to be very small but this gives large I_b. This increase in I_b is offset by a decrease in I_b hence there is not much overall improvement in stability.

• Output is feedback to the base via R_b and this reduces the net gain of the transistor.

Self-Bias/ Potential Divider/ Emitter Bias

• As compared to collector-base bias, if the load of the collector is a transformer, then R_c will be small so $\beta R_c >> R_b$ cannot be achieved. But self-bias is suitable for any type of load resistance.

• Emitter bias is applied by a resistor R_s between the emitter and ground i.e, Thevenin equivalent of two resistor of self bias.

• When collector current increased the voltage drop across R_c increases and reduce forward bias V_{be} reducing base current I_b and keeping the operaing point stable.

• Stability factor

$$S = \frac{1+\beta}{1+\frac{\beta R_c}{R_b + R_c}}$$

• $R_e >> R_b$, S = 1 Best stability

• R_e introduces both dc and ac feedback.

• In order to avoid the loss of ac signal gain because of feedback caused by Re. This R_e is by passed by a leakage capacitor C_e of high value so that is offering little resistance at frequency of interest.

$$S_\beta = \frac{\delta I_c}{\delta \beta} \quad ; \quad S_\beta = \frac{I_{C1} \cdot S_2}{\beta_1(1+\beta)}$$

$$S_v = \frac{\delta I_c}{\delta V_{be}} \quad ; \quad S_v = \frac{\beta}{R_b + R_c(1+\beta_2)}$$

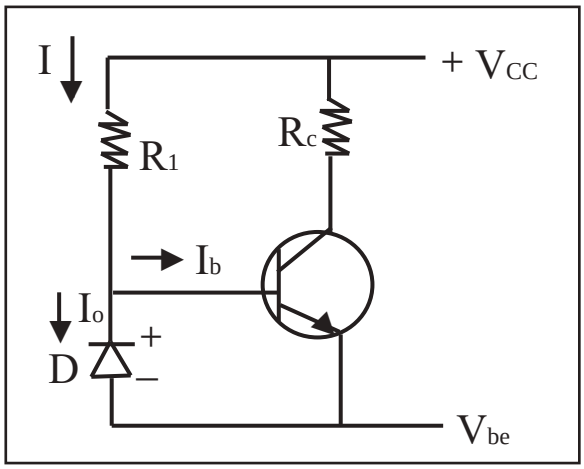
where S_2 : Stability (S) at $\beta = \beta_2$

Total increment in I_c is the sum of all there increaments due to I_{co}, β and V_{be}

$\Delta I_c = S_1 .\Delta I_{co} + S_v . \Delta V_{be} + S_\beta \Delta\beta$

Compensation Techniques

- Major disadvantage of the resistor biasing techniques is the feedback of the output signal to input which causes reduction in gain. To avoid this, compensation technique with diodes, transistor and Thermsitor are employed.
- Diode compensation.



- Reversed biased diode is connected in the base emitter circuit, which is same material as transistor.
- The reverse bias voltage V_{be} allowing the reverse saturation current to I_o to flow through the diode D.

$$I = \frac{V_{cc} - V_{be}}{R_l} = \frac{V_{cc}}{R_l}$$

And $I_B = I - I_o$

From collector current expression

$I_c = \beta I_b + (1 + \beta) I_{co} = \beta I - \beta I_o + (1 + \beta) I_{co}$

$= \beta I - \beta I_o + \beta I_{co}$ if $\beta >> 1$ and I_o of diode and I_{co} of transistor track each other over the desired temperature rang, then I_{co} remains essentially constant. Reverse saturation current I_o flows through the diode. If I_{co} increases due to temperature, the increased current flows through diode decreasing I_b keeping I_b constant.

Thermistor

Thermistors are temperature sensitive element, which has a negative temperature coefficient of resistance.

The thermistor element is placed parallel to and across V_{cc} and E. R_2 of potential divider bias. Increase of temperature reduces resistance and decrease the forward bias reduces I_b and I_c.

Sensistor Compensation

It may be placed either in parallel with R_1 or parallel with R_E. It can also be placed in place of R_E rather than in parallel with R_E.

FET/ MOSFET Biasing

For the field effect transistor, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation. The non linear relationship between I_D and V_{GS} can complicated the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the analysis of all FET amplifiers are

$$I_G \approx 0\ A \quad \text{and} \quad I_D = I_S$$

For JEETS and depletion type MOSFET's Shockley's equation is applied to relate the input and output quantities :

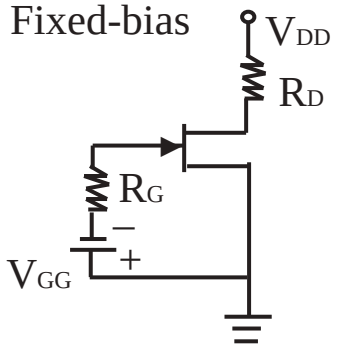
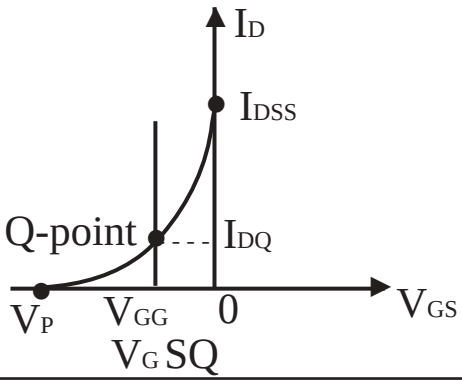
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For Enhancement MOSFET

$$I_D = k(V_{GS} - V_r)^2$$

It is particularly important to realize that of the equations above are for the device only. They do not change with each network configurations. So long as the device is in the actuve region.

Table : FET Bias Configurations

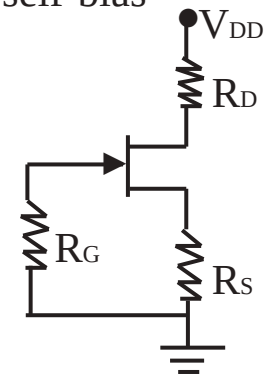
Type/configuration/ pertinent equations	Graphical solution
JFET Fixed-bias 	

$I_G \cong 0$

$V_{GS} = - V_{GG}$

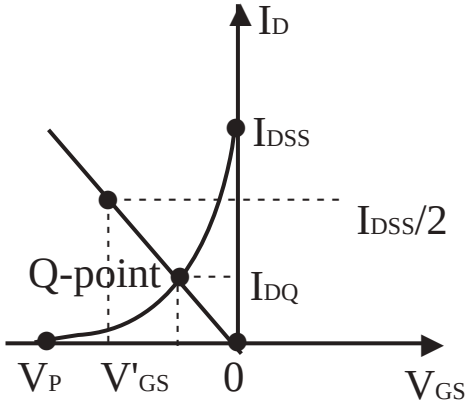
$V_{DS} = V_{DD} - I_D R_S$

JFET self-bias



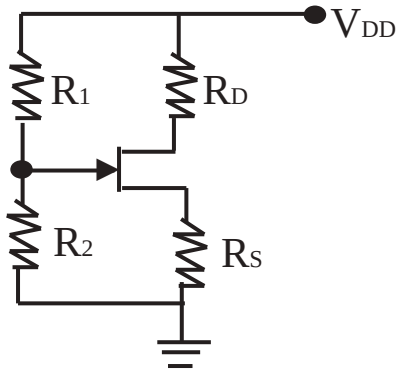
$V_{GS} = - I_D R_S$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$



$V_{GS} = - \frac{I_{DSS} \cdot R_S}{2}$

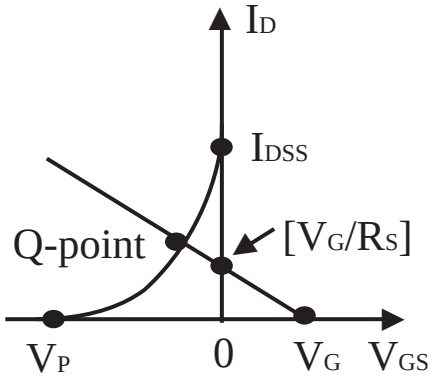
JEFT/ Voltage-divider bias



$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

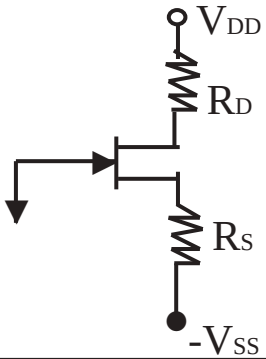
$V_{DS} = V_{DD} - I_D (R_D + R_S)$

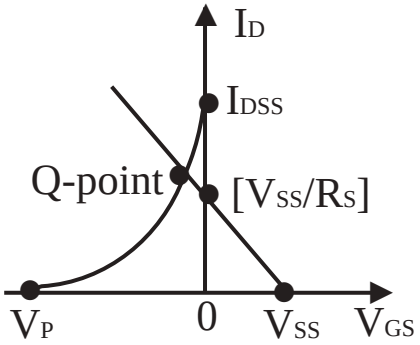


$V_D = V_{DD} - I_D R_D$

$V_S = I_D R_D$

JFET/common gate



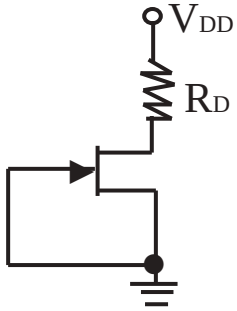


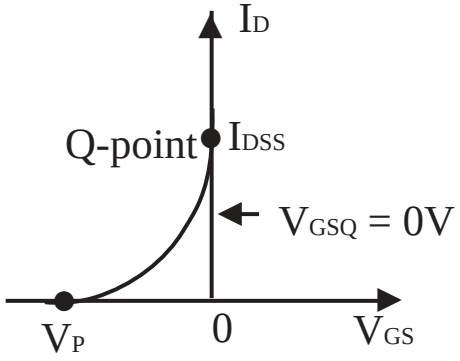
$V_{GS} = V_{SS} - I_D R_S$

$V_{DS} = V_{DD} + V_{SS}$

$= - I_D (R_D + R_S)$

JFET ($V_{GSQ} = 0$ V)

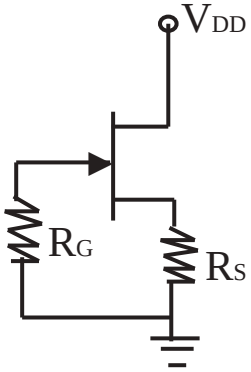


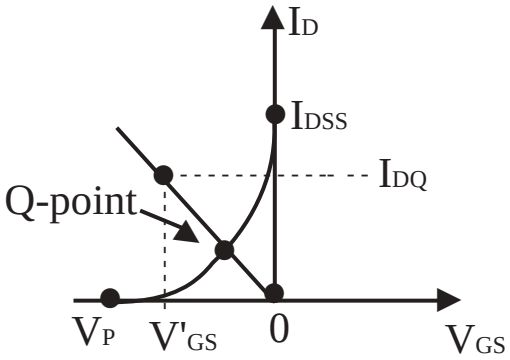


$V_{GSQ} = 0$ V

$I_{DQ} = I_{DSS}$

JFET ($R_D = 0\Omega$)





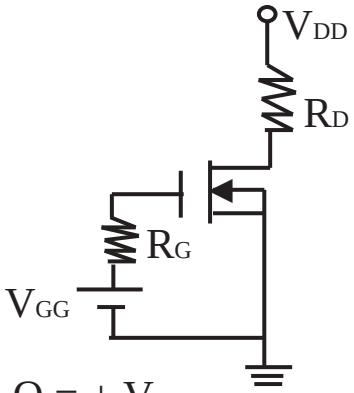
$V_{GS} = - I_D R_S$

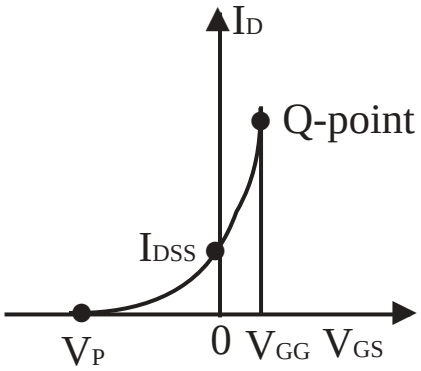
$V_D = V_{DD}$

$V_S = I_D R_S$

$V_{DS} = V_{DD} - I_S R_S$

Depletion type MOSFET/ fixed-bias

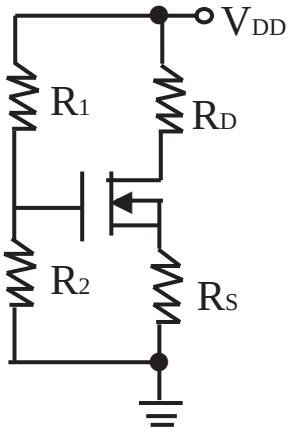




$V_{GS}\,Q = + V_{GG}$

$V_{DS} = V_{DD} - I_D R_S$

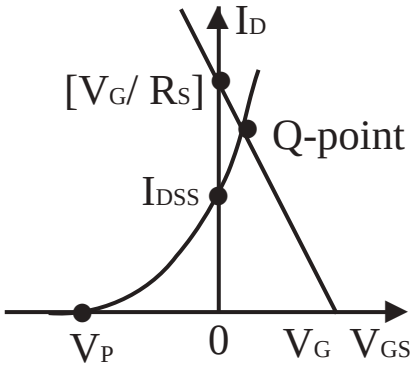
Depletion-type
MOSFET/ voltage-divider bias



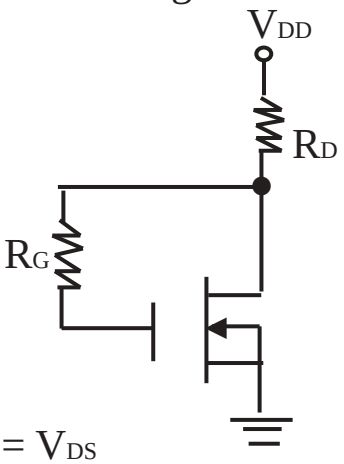
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$V_{GS} = V_G - I_S R_S$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$



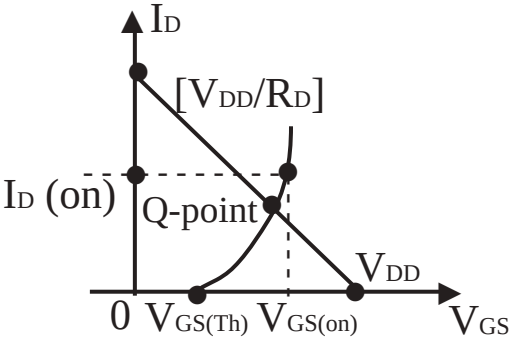
Enhancement type MOSFET/
feedback configuration



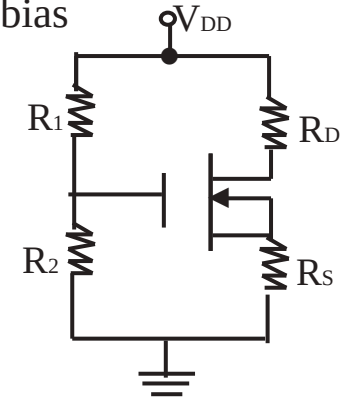
$V_{GS} = V_{DS}$

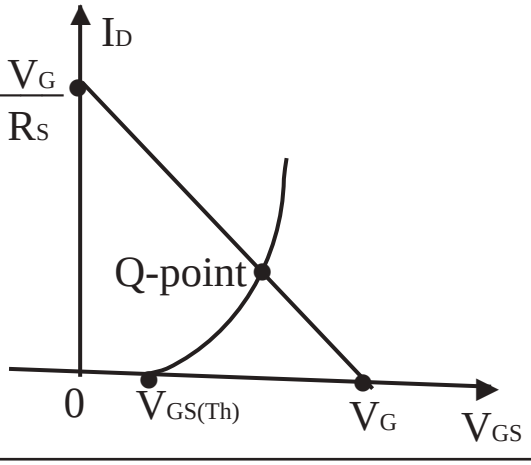
$V_{GS} = V_{DD} - I_D R_D$

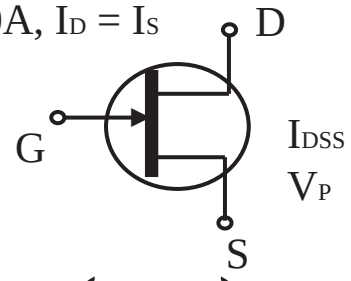
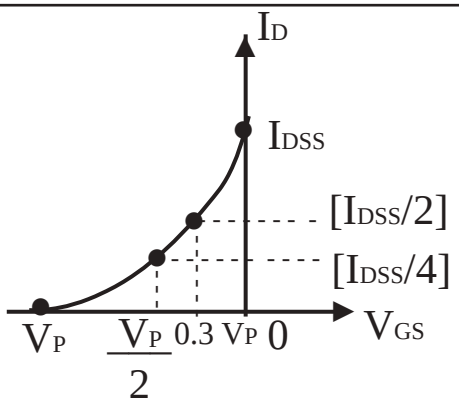
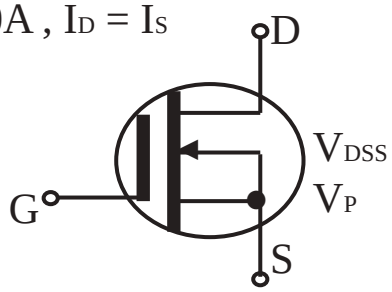
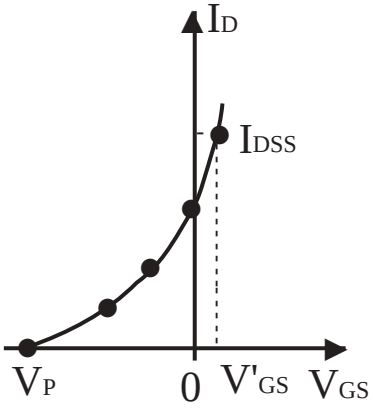
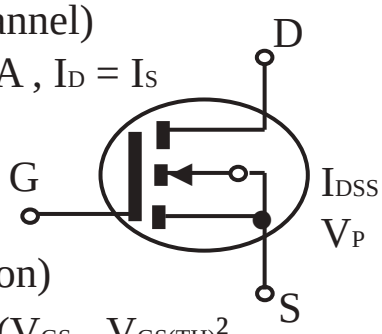
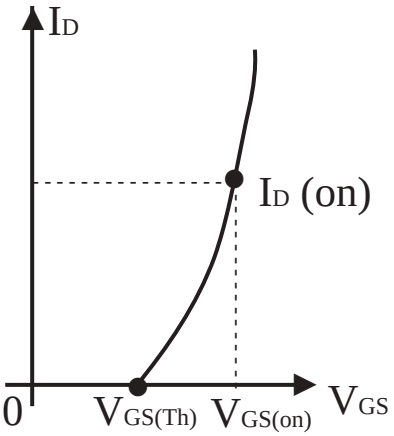
$I_D = k[V_{GS} - V_{GS(tw)}]^2$



Enhancement type MOSFET/ voltage
Divider bias

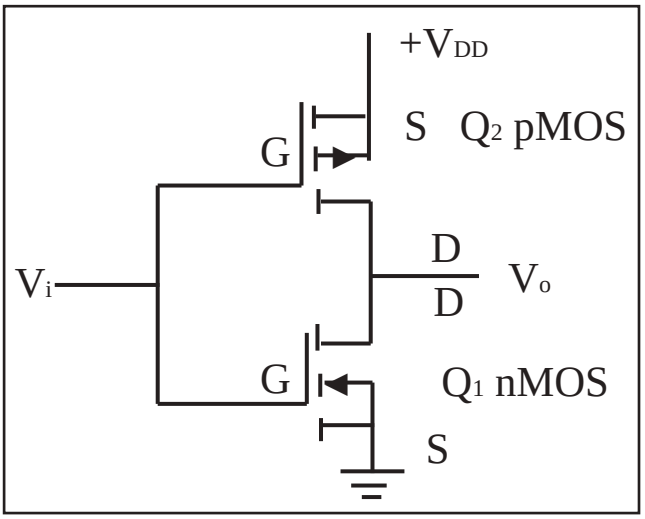




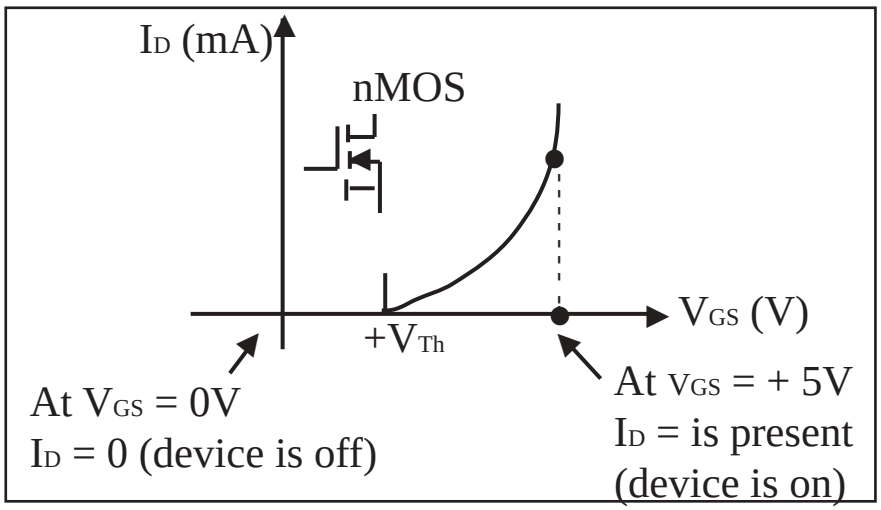
$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	
Type/Symbol/ Basic relationships	Transfer curve input resistance capacitance
JFET (n-channel) $I_C = 0A, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	 $R_i > 100\ M\Omega$ C_i : (1 - 100) pF
MOSFET depletion- type (n-channel) $I_G = 0A , I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	 $R_i > 10^{10}\ \Omega$ C_i (1 - 10) pF
MOSFET enhancement type (n-channel) $I_G = 0A , I_D = I_S$  V_{GS} (on) $I_D = k(V_{GS} - V_{GS(TH)}^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$	 $R_i > 10^{10}\ \Omega$ C_i (1 - 10) pF

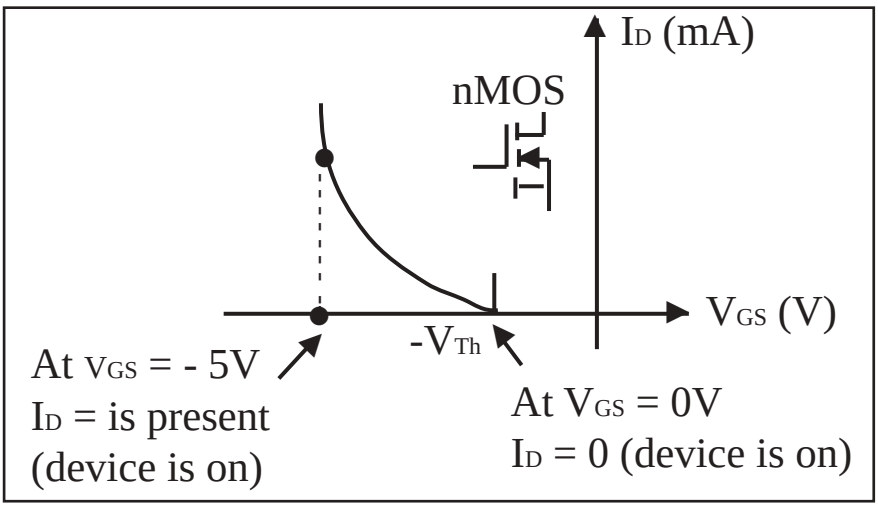
CMOS Biasing

A form of circuit popular in digital circuitry uses both n-channel and p-channel enhancement MOSFET transistor. This complementary MOSFET or CMOS circuit uses these opposite (or complementary)-type transistors. The input, V_i is applied to both gates with the output taken from the connected drains.



An input of 0V leaves the nMOS off, while an input of +5 V turns the nMOS on.





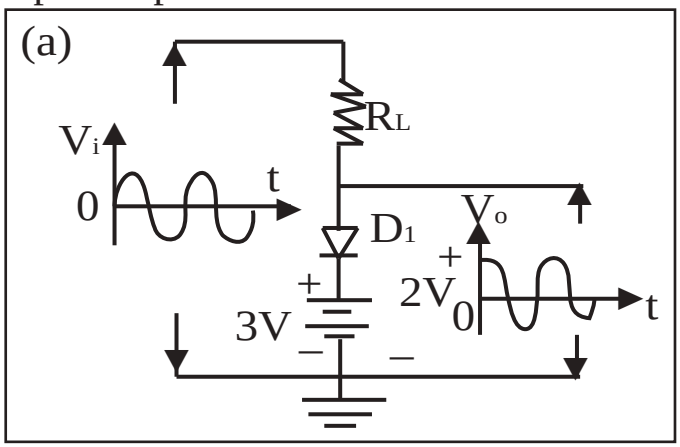
V_{GS} = 0V leaves pMOS off : V_{GS} = -5V turns pMOS on.

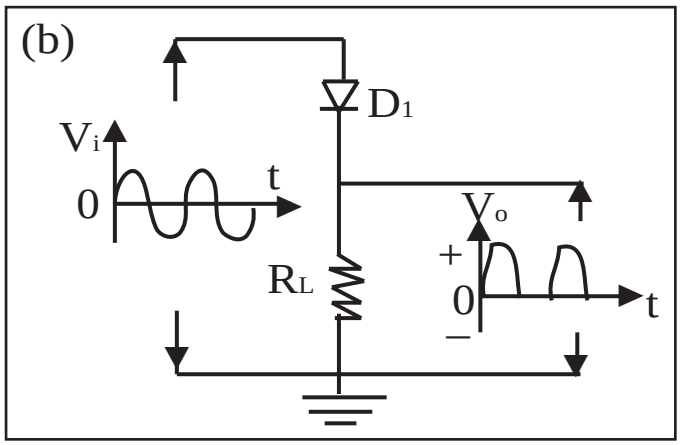
Operation of CMOS circuit			
V_i (V)	Q_1	Q_2	V_o (V)
0	Off	On	+5
+5	On	Off	0

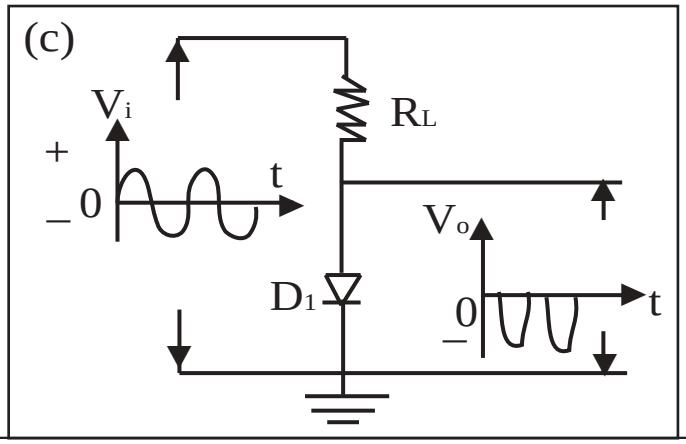
Diode Circuits

Diode Clipping Circuits

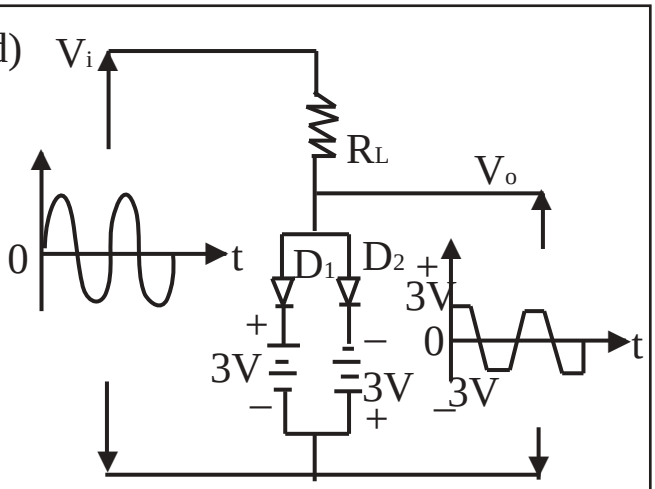
Clipping circuit are used to select for transmission that part of an arbitrary wave form which lies above or below some particular reference voltage level. These are also called voltage or current limiters. Some typical clipping with input output waveform are shown.



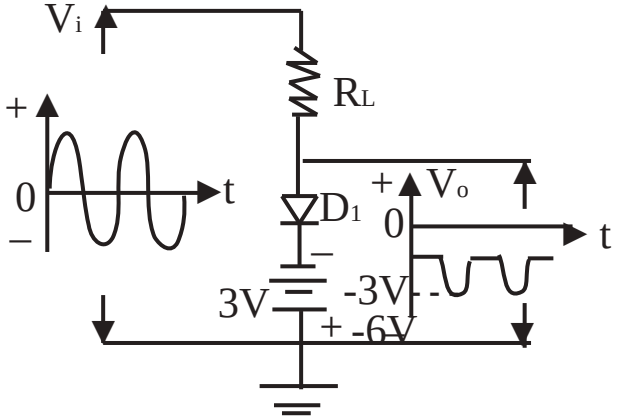




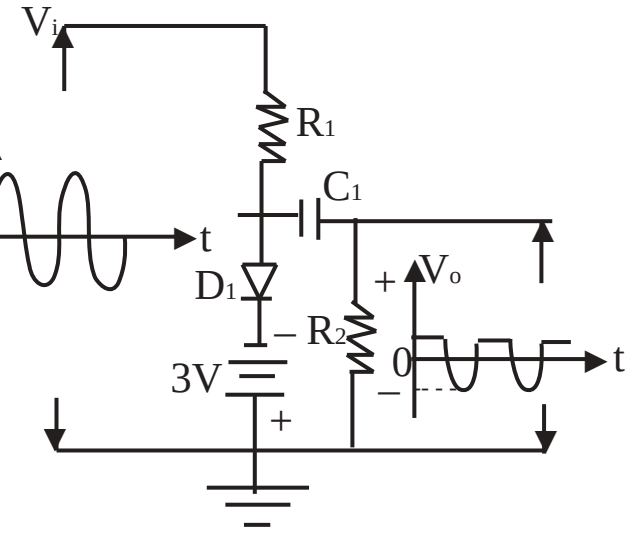
(d)

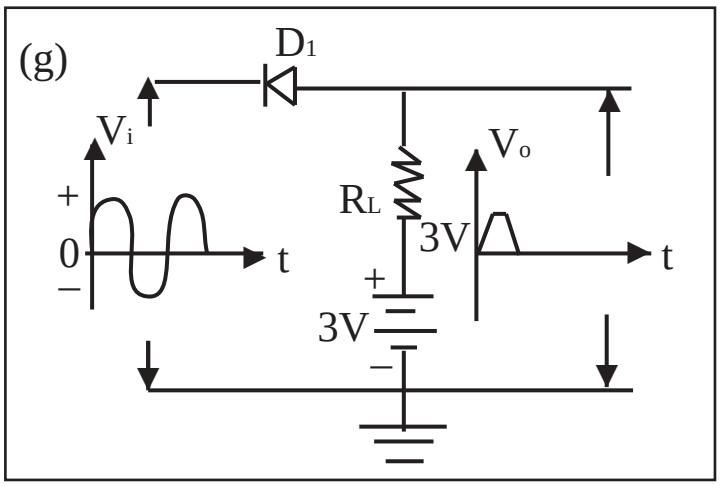

Vi
RL
Vo
0
t
D1
D2
+
3V
0
t
+
–
3V
3V
–3V
–
+

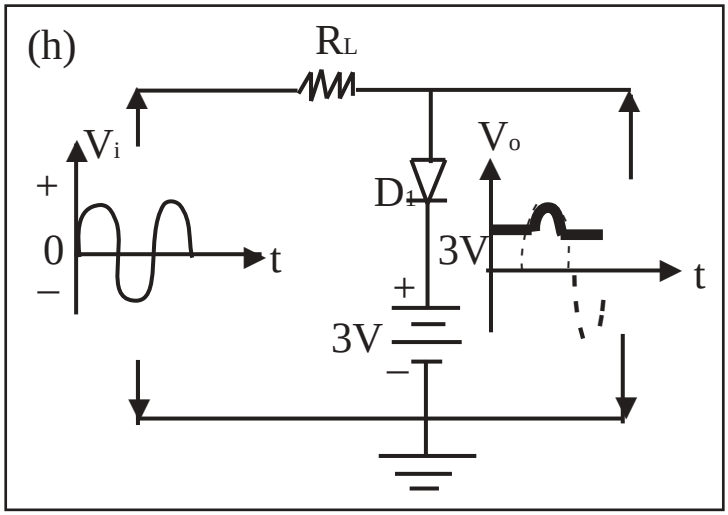
(e)


Vi
RL
+
0
t
–
+
Vo
D1
0
t
–
3V
-3V
+ -6V

(f)


Vi
R1
C1
0
t
D1
+
Vo
– R2
0
t
3V
+





Diode Clamping Circuits

The clamping circuit establisher a recurrent positive or negative extremity at some constant reference voltage level VR. The clamping circuit introduces a d.c component to a waveform that has lost its dc component after passing through a capacitive coupling network. For the reason, clamping circuit is often referred to as dc restorer or dc inverter.

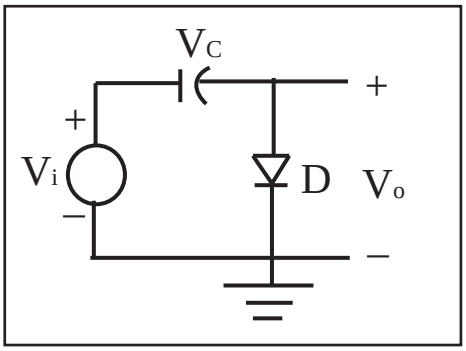
In some situation it may be necessary to raise or lower reference voltage, which is done by adding or subtracting a dc voltage to the original reference voltage of 0.

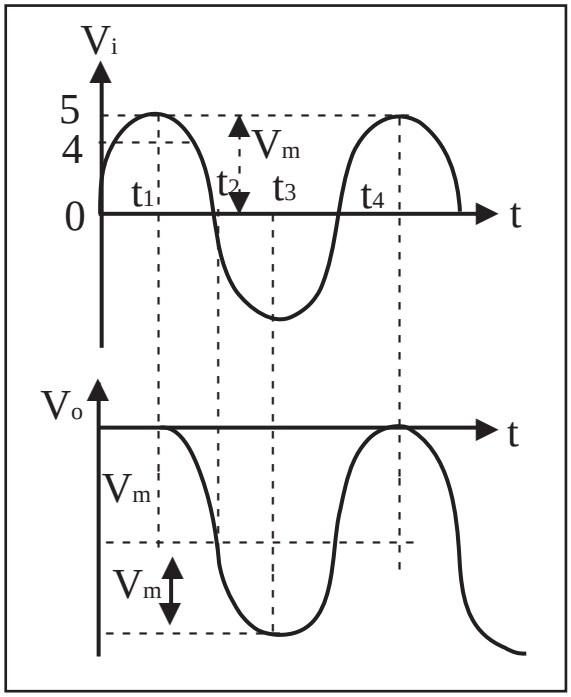
Two Type of Clamper Circuit :

(a) If the d.c level added is positive , it is positive clamper.
(b) If the d.c level is lowered and negative, it is negative clamper.

Negative Clamper

Consider the given circuit which consist of signal source V_i of neglecting output impedance a capacitor and diode D.





Assuming the ideal diode i.e $V_y = 0$ and $R_f = 0$. The input is sinusoidal. During first quarter cycle of input signal the capacitor get charged as the diode is forward biased, no output voltage.

$\therefore V_o = 0$

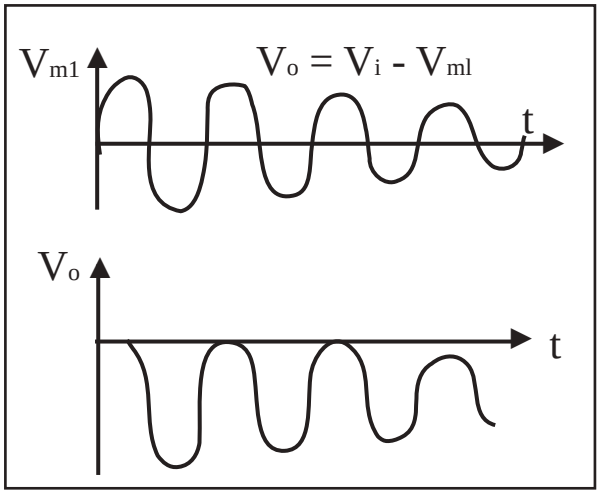
At the end of first quarter cycle $V_c = V_m$. After the diode comes reverse bias. The input signal reduces but the capacitor is not able to discharge due to diode.

$$V_o = V_i - V_m$$

During suceeding cycles the positive excusion of the signal just barely reaches zero. The diode need never again conduct and the positive extremity of the signal has been clamped or restore to zero.

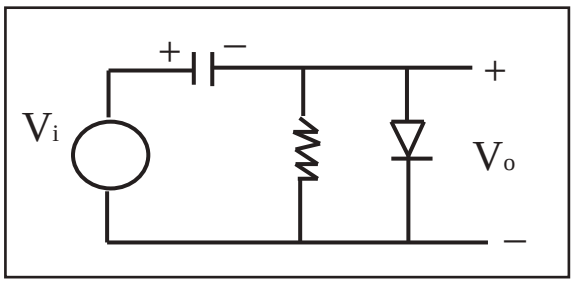
If the amplitude of the input signal increases, the diode will conduct for first quarter cycle. The capacitor will again get charged and positive extremity will get clamped to zero voltage.

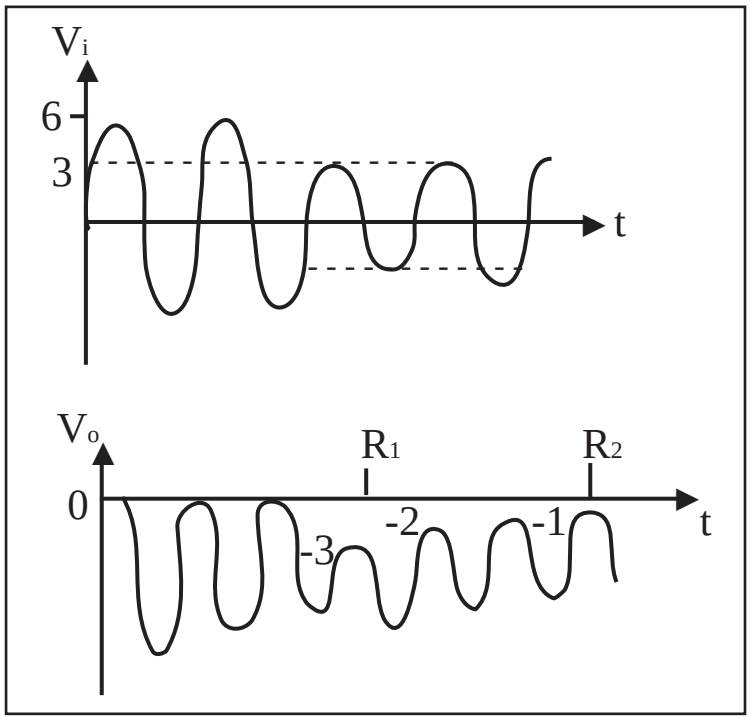
However, if the amplitude of input signal decrease. The signal does not remain clamped to zero. The reason being that capacitor does not get path to discharge.



To permit a decrease in capacitor voltage it is necessary to shunt a resistor across c or to shunt a resistor across the diode.

The circuit with shuntting diode is given below.





Now the capacitor get a discharge path. When the input suddenly rate.

$V_o = V_i \rightarrow V_{ml}$

Even if the input does not decrease to 3V the capactior continues to discharge and diode get forward bias during the peak of input voltage capacitor charge

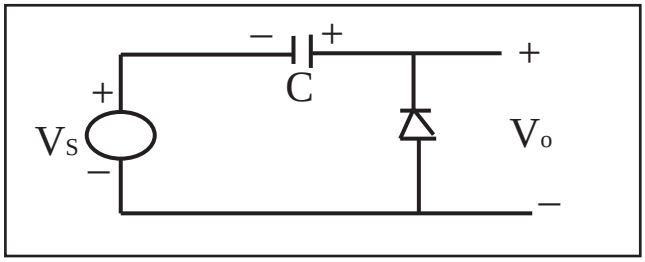
during peaks. The RC time constant is very important. It must be very large in comparison with the period of signal.If it become if capacitorlosses too much of charge when diode is not conducting, then it may be that it does not charge during the small time interval when diode conduct.

Clamping circuit taking source and diode resistance into account.

The realistic clamping circuit is given below :

Here source resistance R_S and diode forward resistance takes into account.

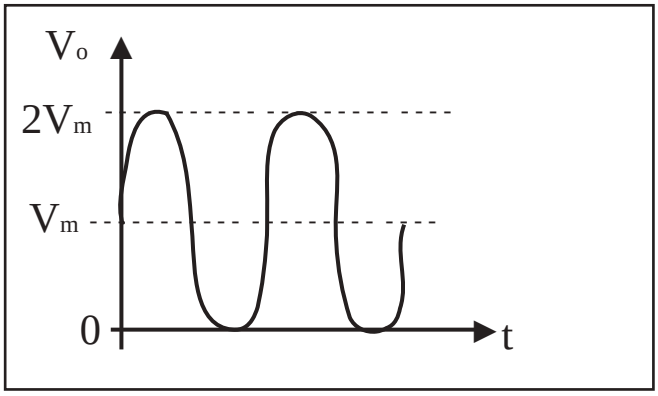
Positive Clamper



$V_s = V_m \sin wt$, for negative swing D conducts and capacitor charge to peak value V_m and cathode end of capacitor is positive.

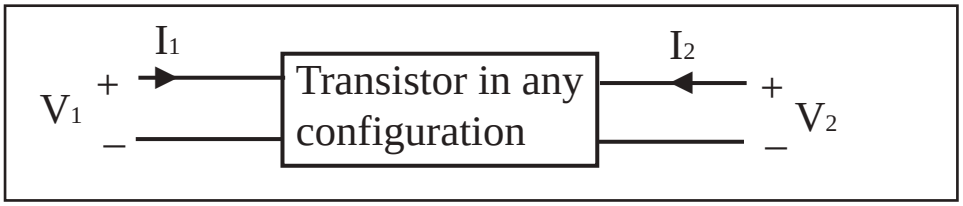
$V_o = V_s + V_c$ (or V_m)

$= 2 Vm$ for positive swing and 0 for negative swing



Transistors at Low and High Frequencies

Hybrid Model : H-Para meter Model



$V_1 = h_{11} I_1 + h_{12} V_2$

$I_2 = h_{21} I_1 + h_{22} V_2$

V_1 and $I_2 \rightarrow$ dependent Variable

I_1 and $V_2 \rightarrow$ Independent Variable

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}$$

$$h_i = h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2 = 0}$$

Input impedance when output is short circuit (Ω)

$$h_r = h_{21} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0}$$

Reverse voltage gain when input is open circuit.

$$h_f = h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0}$$

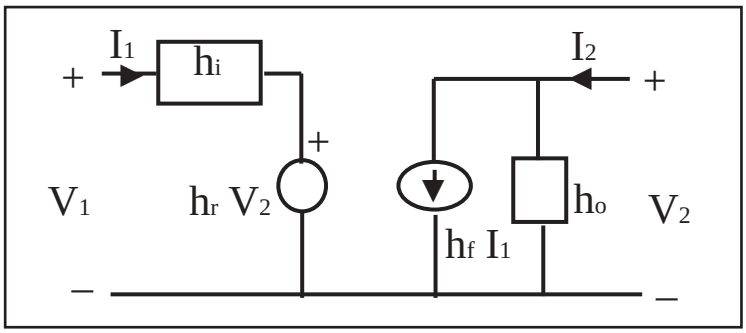
Forward current gain when output is short circuit.

$$h_o = h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0}$$

Output admitance when input is open circuit (s).

$V_1 = h_i I_1 + h_r V_2 \leftarrow$ KVL

$I_2 = h_f I_1 + h_o V_2 \leftarrow$ KCL

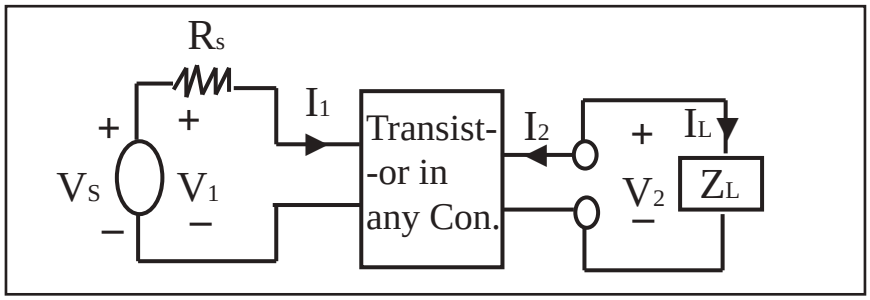


Important Point of Hybrid Model

1. We use h-parameter in the equivalent circuit of a transistor since this parameters are relatively constant (real number) with respect to audio frequency and temperature.
2. We find the h-parameter under different condition, i.e by open circuit the input or short circuit the output. Since these parameter have mixed units, these are called hybrid parameter.
3. For a given configuration of transistor the form h-parameter are always specified by manufactures.
4. They are easy to measure.
5. They can be obtained from the transistor ststic characteristic curves.
6. These are particularly convenient to use in the circuit analysis and design.
7. There parameter hold good for any configuration specified type of transistor

that in NPN or PNP, Si or Ge at low frequency.

General Analysis of Transistor Amplifier



$V_1 = h_i I_1 + h_r V_2$

$I_2 = h_f I_1 + h_o V_2$

Current gain (A_1)

$$A_1 = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

$I_2 = h_f I_1 + h_o V_2$

Divide the above equation by I_1

$$\frac{I_2}{I_1} = h_f + h_o \left(\frac{V_2}{I_1}\right) \qquad (1)$$

Now $V_2 = I_L Z_L = - I_2 Z_L$ (2)

From equation (1) and (2)

$$\frac{I_2}{I_1} = h_f + h_o \left(\frac{-I_2 Z_L}{I_1}\right)$$

$$\frac{I_2}{I_1} (1 + h_o Z_L) = h_f$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o Z_L}$$

$$A_1 = -\frac{I_2}{I_1} = \frac{- h_f}{1 + h_o Z_L}$$

Input impedance (Z_{in})

$Z_{in} = [V_1 / I_1]$

$V_1 = h_i I_1 + h_r V_2$

Divide the above equation by I_1

$$\frac{V_1}{I_1} = h_i + h_r \frac{V_2}{I_1} = h_i + h_r \left(\frac{-I_2 Z_L}{I_1}\right)$$

Put the value of V_2 from equation (2)

$Z_{in} = - h_i + h_r . A_1 Z_L$

Volatge gain (A_v)

$A_v = [V_2 / V_1]$

Put the value of equation (2)

$V_1 = I_1 Z_{in}$

$A_v = \frac{-I_2 Z_L}{I_1 Z_{in}}$; $A_v = \frac{A_1 Z_L}{Z_{in}}$

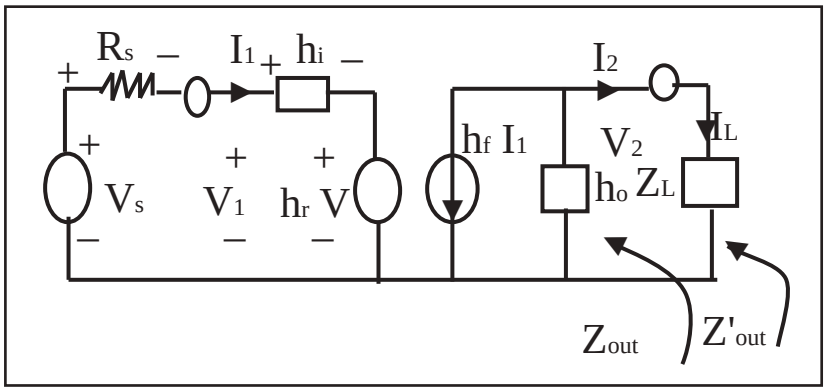
Output impedance Z_{out}

$Z_{out} = \left.\frac{V_2}{I_2}\right|_{V_s = 0}$

$I_2 = h_f I_1 + h_o V_2$

Divide the above equation by V_2

$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$ (3)



KVL at input :

$-V_s + I_1 (R_s + h_i) + h_r V_2 = 0$

$0 + I_1(R_s + h_i) = -h_r V_2$

$\frac{I_1}{V_2} = \frac{-h_f}{R_s + h_i}$ (4)

From equation (3) and (4)

$\frac{I_2}{V_2} = h_f \left(\frac{-h_f}{R_s + h_i}\right) + h_o$

$Z_{out} = \left[h_o - \frac{h_f h_r}{(R_s + h_i)}\right]$ $Z'_{out} = Z_{out} \parallel Z_L$

Power gain $A_P = A_v \cdot A_1$

Voltage gain taking R_S into account i.e overall voltage gain

$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} = A_v \left(\frac{V_1}{V_s}\right)$

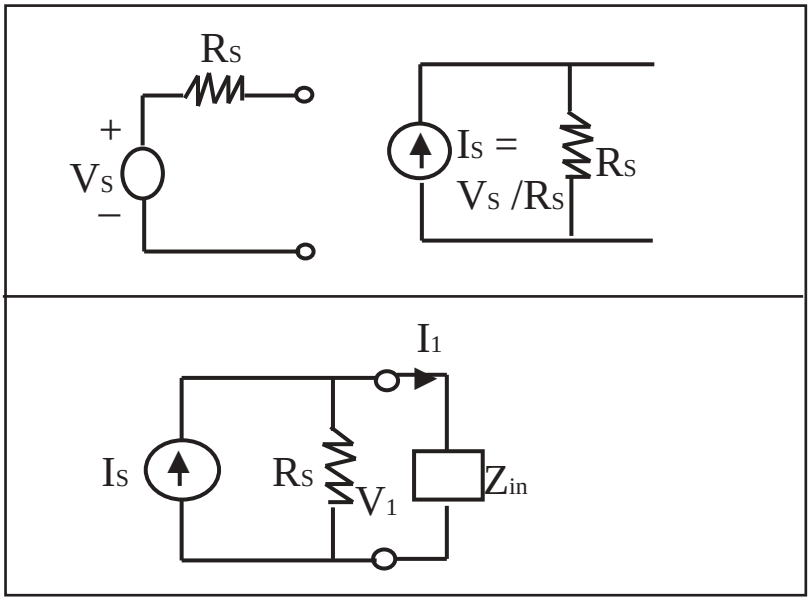
$\frac{V_1}{V_s} = \frac{Z_{in}}{Z_{in} + R_s}$

$A_{vs} = A_v \left[\frac{Z_{in}}{Z_{in} + R_s}\right]$ $\Rightarrow A_{vs} < A_v$

$A_{vs} = A_v$ => when $R_s = 0$

Current gain taking R_s into account i.e overall current gain

$$A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_1} \times \frac{I_1}{I_S} = A_1\left(\frac{I_1}{I_S}\right)$$



$$\frac{I_1}{I_s} = \frac{R_s}{R_s + Z_m}$$

$$A_{IS} = A_I\left[\frac{R_s}{R_s + Z_{in}}\right] \quad A_{IS} < A_I$$

$A_{IS} = A_I$ when $R_S = \infty$

=> Ideal current source

Overall power gain

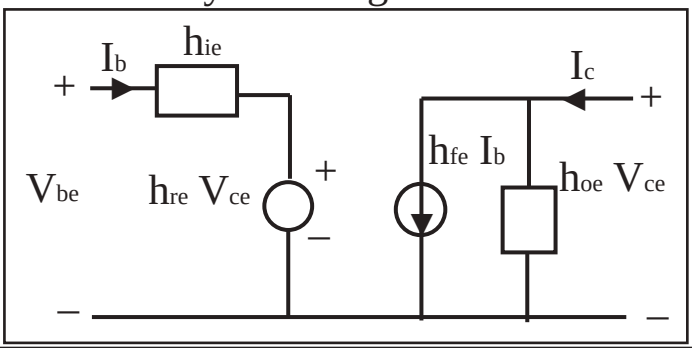
$A_P = A_{VS} \times A_{IS}$

Approximate Analysis of Transistor

In general for a transistor if

1. $h_{oe} = 10^{-6}$ S
2. $h_{re} = 10^{-4}$
3. $h_{oe} Z_L \leq 0.1$

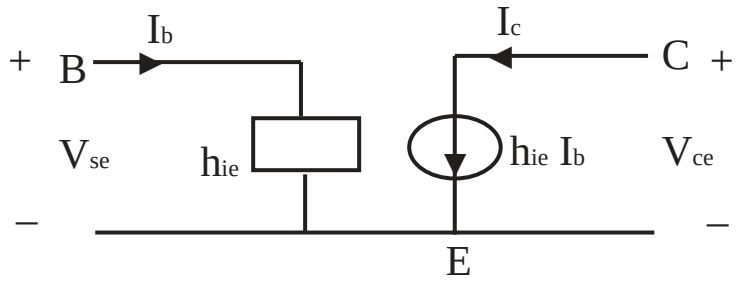
Then it is seen that the error made in the analysis is < 10%, in such case approximate analysis hold good for CE.



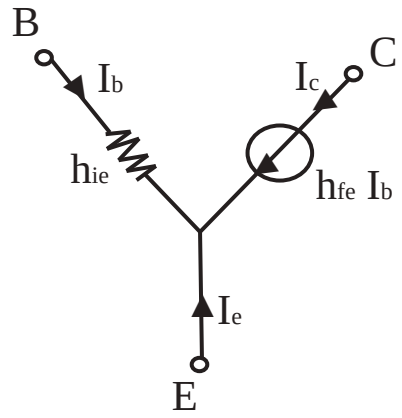
$h_{re} = 10^{-4}$ neglected voltage source $h_{rc}\ V_{ce}$ is short circuit.

$h_{oe} = 10^{-6}$

S => $(1/h_{oe})$ is large which draw negligible current i.e. open circuit.



Approximate CE circuit is simplified as

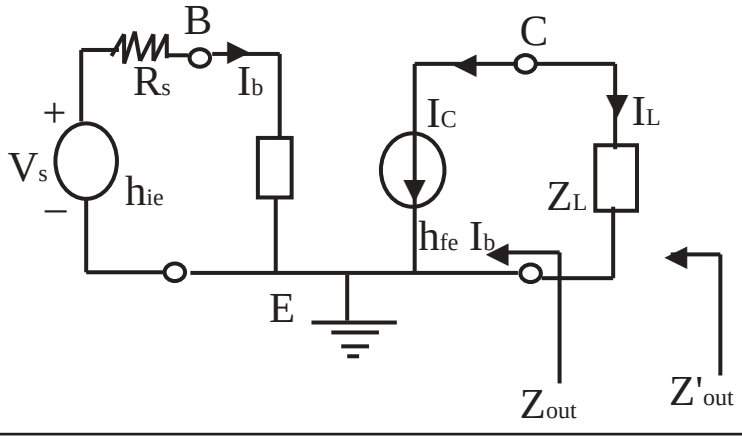


Approximate h-model which may be used for all three configuration

$h_{re} = 10^{-4}$ $h_{oe} = 10^{-4}$ S

$h_{fe} = 100$ $h_{re} = 2k$

CE Analysis



1. $A_I = \frac{I_L}{I_b} = \frac{-I_C}{I_b} = \frac{-h_{fe}\ I_b}{I_b} = h_{fe}$ phase inversion

2. $Z_{in} = \frac{V_{be}}{I_b} = \frac{-h_{ie}\ .\ I_b}{I_b} = h_{ie} \cong 1\ k\Omega$

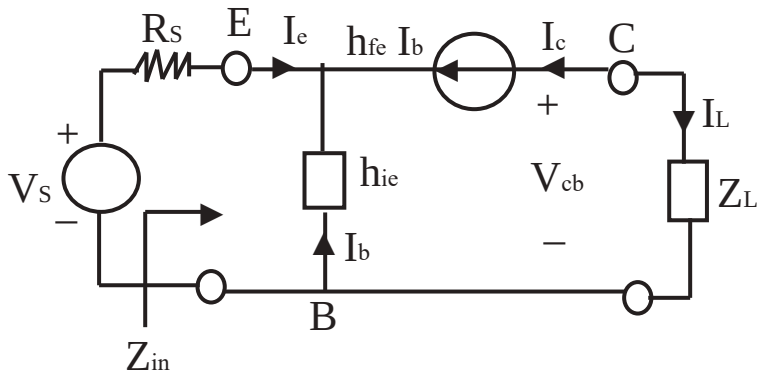
3. $A_v = \frac{A_1}{Z_{in}} Z_L = - h_{fe} \frac{Z_L}{h_{ie}}$

4. $Z_{out} = \infty$; due to idle current source

$Z'_{out} = Z_{out} \,||\, Z_L = \infty \,||\, Z_L = Z_L$

1. The current gain is high (h_{fe})
2. Voltage gain is high
3. Input and output current are out of phase by 180º.
4. The input and output voltage are out of phase by 180º.
5. Input impedance is medium.
6. Output impedance is medium.
7. Since volatge gain and current gain both are simultaneously high, this configuration is always used as an amplifier.

CB Analysis



1. Current gain

$$A_I = \frac{I_L}{I_e} = \frac{-I_c}{I_e}$$

$$= \frac{-h_{fe} I_b}{-(1 + h_{fe}) I_b} = \frac{h_{fe}}{1 + h_{fe}} = \frac{\beta}{1 + \beta} =< 1$$

2. $Z_{in} = \frac{V_{eb}}{I_e} = \frac{-h_{ie} I_b}{-(1 + h_{fe}) I_b} = \frac{h_{ie}}{1 + h_{fe}}$ => very low

3. $A_v = A_1 \frac{Z_L}{Z_{in}} = \left(\frac{h_{fe}}{1 + h_{fe}} \right) \times \frac{Z_L}{\left(\frac{h_{ie}}{1 + h_{fe}} \right)} = \frac{h_{fe} \,.\, Z_L}{h_{ie}}$

4. $Z_{out} = \infty$

$Z_{out} = \infty \,||\, Z_L = Z_L$ => highest

$$Z_{out} = \frac{V_{eb}}{I_c}\Big|_{V_s = 0} = \frac{V_{eb}}{0} = \infty$$

$V_s = 0$; 1 $I_c = 0$

Feature

1. Low current gain (α) => always less than 1.
2. High voltage gain (approximately equal CE).
3. Input and output current are in phase.
4. Input and output voltage are in phase.
5. It has lowest input impedance of all three configurations.
6. It has highest output impedance of all three configurations.
7. Since, current gain is approximately equal 1, it can be used as constant current source.
8. Can be used at place where transformation of impedance from a very low value of very high value to desired.
9. Non-inverting amplifier with $A_V > 1$ and $A_I < 1$.

1. $A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b} = \frac{(1 + h_{fe})I_b}{I_b} = 1 + h_{fe}$

2. $Z_{in} = \frac{V_{bc}}{I_b} = \frac{h_{ie} \cdot I_b + I_L Z_L}{I_b}$

$$= \frac{h_{ie} I_b + Z_L (1 + h_{fe})I_b}{I_b}$$

$Z_{in} = h_{ie} + (1 + h_{fe})Z_L$ => highest

3. $A_v = A_I \frac{Z_L}{Z_{in}} = \frac{(1 + h_{fe})Z_L}{h_{ie} + (1 + h_{ef}) Z_L} = \frac{x}{h_{ie} + x}$ (<1)

where $x = (1 + h_{ef}) Z_L$

4. $Z_{out} = \left.\frac{V_{ec}}{I_e}\right|_{V_s = 0}$

$V_{ec} = -h_{ie} I_b - R_s I_b + V_s = -(h_{ie} + R_s)I_b$

$I_e = -(1 + h_{fe})I_b$

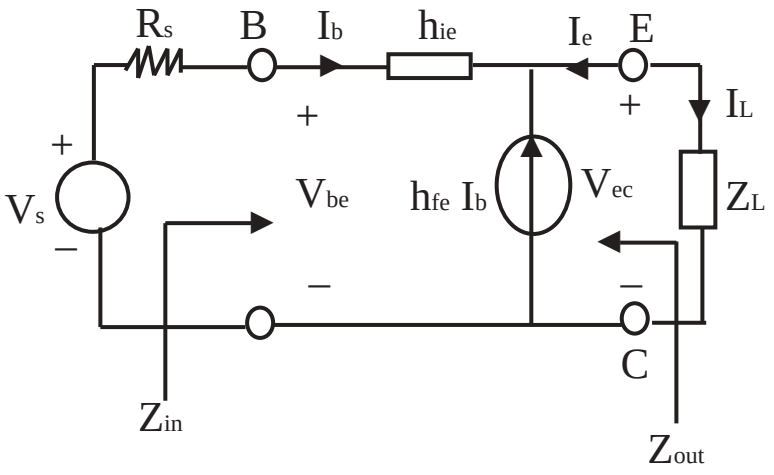
$Z_{out} = \frac{h_{ie} + R_s}{(1 + h_{fe})}$ => lowest

Feature

1. Highest current gain $(1 + h_{fe})$.
2. Voltage gain always less the unity (lowest).
3. Input and output current are in phase.
4. Input and output voltage are in phase.
5. Input impedance is the highest of all the three configurations.
6. Output impedance is the lowest of the three configurations.

7. Used at place where the impedance conversion from a high value to low valueis desired. Therefore it is always used as last stage of any audio amplifier where its output impedance is matched to low impedance speaker to transfer maximum amount of power.

CC / Emitter Follower



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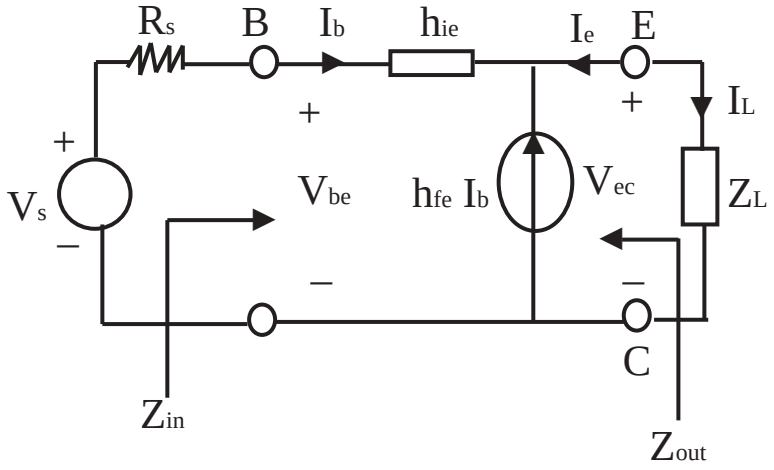
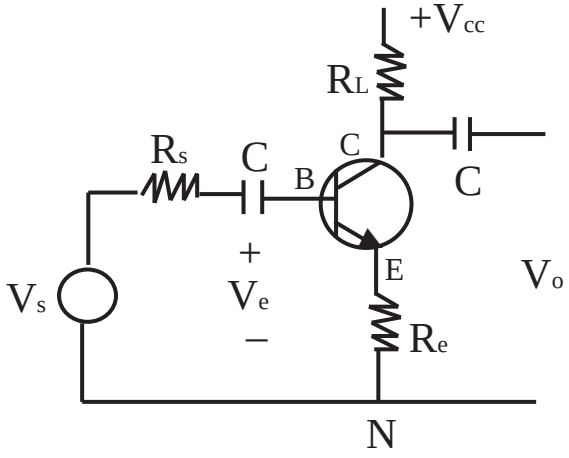
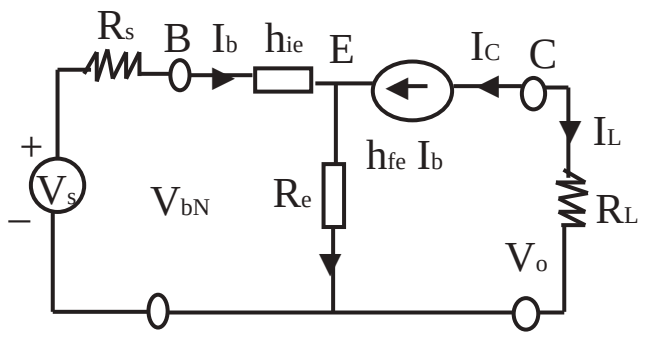
CC / Emitter Follower



8. Since it is having high input impedance therefore it can be used as a buffer amplifier, which draw negligible current and does not load the previous stage.
9. Z_{in} depend upon the load.

CE Amplifier with Emitter Resistance R_E





It is very important to stabilize the voltage amplification of an amplifier, i.e. it becomes independent or h-parameter.

$$I = I_b + h_{fe} I_b = (1 + h_{fe}) I_b$$

2. $A_I = \frac{I_L}{I_b} = \frac{-h_{fe} I_b}{I_b} = - h_{fe}$ => unaffected

3. $Z_{in} = \frac{V_b}{I_b} = \frac{h_{ie} I_b + R_e I}{I_b}$

$$= \frac{h_{ie} I_b + (1 + h_{fe}) I_b \cdot R_e}{I_b}$$

$$= h_{ie} + (1 + h_{fe}) R_e$$

Z_{in} increased by a factor of $(1 + h_{fe}) R_e$

4. $A_v = A_I \cdot \frac{Z_L}{Z_{in}}$

$$= \frac{-h_{fe} \cdot R_L}{h_{ie} + (1 + h_{fe}) R_e}$$ => decreased

5. $Z_{out} = \infty$

$Z_{out} = \infty \mid\mid R_L = R_L$

Comparison with Ce Amplifier

1. The current gain and output impedance remain unchanged.
2. The input impedance is increased by the amount $(1 + h_{fe})R_e$ .. .. this is advantage.
3. The voltage gain decreased by the amount $(1 + h_{fe})R_e$.

$$A_v = \frac{-h_{fe} \cdot R_L}{h_{ie} + (1 + h_{fe}) R_e}$$ as $h_{fe} >> 1$

$$\text{then} = \frac{-h_{fe} \cdot R_L}{h_{ie} + h_{fe} \cdot R_e} = \frac{-h_{fe} \cdot R_L}{h_{fe} \cdot R_e} = \frac{-R_L}{R_e}$$

Let, $h_{fe} R_e >> h_{ie}$ . . . . . practically

$A_v = - \frac{R_L}{R_e}$ i.e. voltage gain is independent of h-parameter.

The h-parameter of transistor vary with respect to temperature so that the voltage gain changes with respect to temperature. Hence since the voltage gain is independent of h-parameter therefore the voltage gain is stabilized against the variation in temperature.

Therefore stability of the circuit increase.

Transistor Parameter value at Low Frequencies

Parameter	CE	CC	CB
h_i	1.1 kΩ	1.1KΩ	20Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51-0.99	
$[1/h_0]$	40 kΩ	40 kΩ	2 MΩ

Approximate values for different quantities using approximate equivalent model are given as follows :

	CB	CC	CE	CE with Re
A_I	$\frac{h_{fe}}{1 + h_{fe}}$	$1 + h_{fe}$	$-h_{fe}$	$-h_{fe}$
Z_{in}	$\frac{h_{ie}}{1 + h_{fe}}$	$h_{ie} + (1 + h_{fe})R_L$	h_{ie}	$h_{ie} + (1 + h_{fe})R_e$
A_v	$\frac{h_{fe} R_L}{h_{ie}}$	$1 - \frac{h_{ie}}{Z_{in}}$	$\frac{-h_{fe} R_L}{h_{ie}}$	$\frac{-h_{fe} R_L}{Z_{in}}$
Z_{out}	∞	$\frac{R_s + h_{ie}}{1 + h_{fe}}$	∞	∞
Z_{out}	R_L	$Z_{out} \mid\mid R_L$	R_L	$\mid R_L$

Amplifiers

Power Amplifier

Power Amplifier are meant for large signal amplification power stage is normally the final stageof a cascade amplifier and driver. The energy conversion device i.e., speaker, antenna or transducer etc. The power amplifier does not actually amplify the power, instead it takes power from the dc power supply connected to the power circuit and converts into use full ac signal power $Z_{in} \rightarrow$ high, $Z_{out} \rightarrow$ low, heat sink are used.

Class A

Here the dc bias is adjusted much less than its cut off value so that output current flow for full input voltage cycle.

Feature :

1. Minimum distortion.
2. Since the output contains only one frequency component, the output power is small.
3. Effeciency is low.
4. Used as voltage amplifier as modulating amplifier.

Class B

Here the dc bias is adjusted equal to the cut off value so that the output current flow foe half of the input voltage cycle. Hence the output dc component will be always equal to zero.

Feature :

1. High distortion.
2. High power output
3. Effeciency is large
4. Used as power amplifier as modulated amplifier.

Class AB

Here the dc bias is adjusted slightly less than cut-off value so that the output current flows for more than half but less than input voltage cycle. This class of amplifier is just a compromise between class A and class B amplifier.

Feature :

1. Output power is medium.
2. Medium distortion.
3. Medium effeciency.
4. Used as modulating amplifier
5. used with unturned power amplifier.

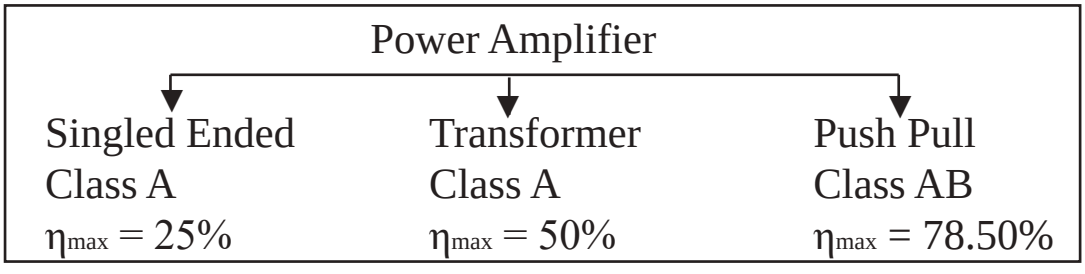
Class C

Here the dc bias is adjusted greater than its cut-off value so that the output current flow for less than half of the input voltage cycle.

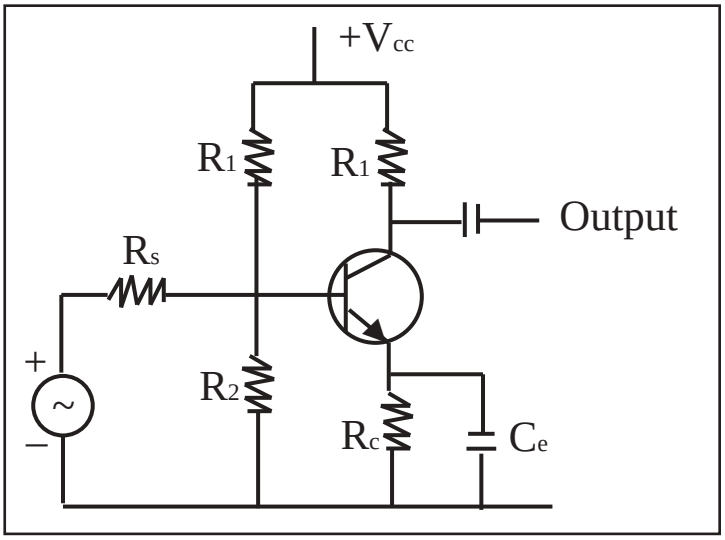
Therefore the output current will be in the form of pulses which will be highly rich in ahrmonic i.e frequency multiplier.

Feature :

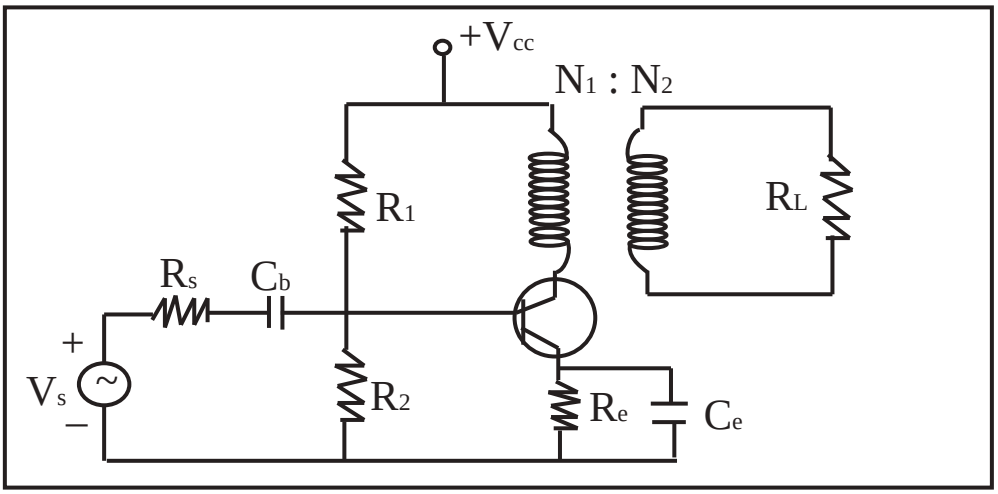
1. Very high output power due to reach in harmonic.
2. Very high distortion.
3. Very high conversion efficiency.
4. Used as only modulated amplifier when the need is to raise the power level before transmission.
5. Used with tuned frequency amplifier.



Single Ended Class A Amplifier



Class A transformer Coupled



Conversion efficiency (η)

$$= \frac{\text{Signal power delivered to load}}{\text{DC power supplied to output circuit}} \times 100 = 50\%$$

[DC power supplied (V_{CC} I_C)]

= AC power developed in load $\left(\frac{1}{2} V_m I_m\right)$

+ power dissipated in load $R_L(I_c^2 R_L)$

+ Dissipation in the Collector P_D

With no signal P_D (max) = V_{CE} . I_C

$\therefore$ P_{ac} delivered = $\frac{1}{2}$ P_D max

This statement is true in both series fed and Transformer coupled cases.

Given P_D max = 20 watts

Then in series fed P_{ac} to load = 10 watts

P_{dc} = 40 watts (η = 25%)

In transformer coupling with P_D max = 20 watts

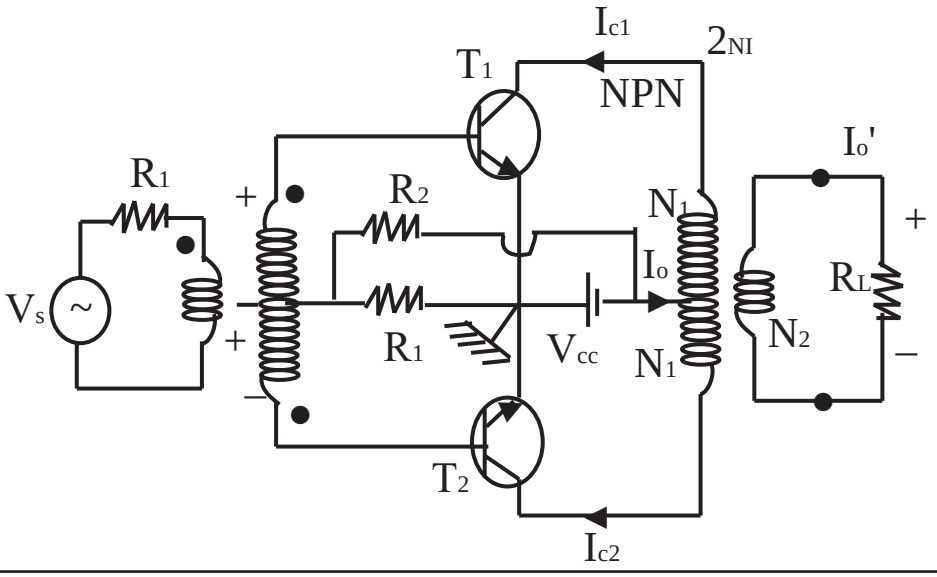
P_D = 20 watts (η = 50%)

Since only 25% ac power is useful at the power output.

η_{max} = 25%

1. Effeciency is very low. This is become of the fact in the large amount of dc power is dissipated across the load.
2. The effeciency can be increased to 50% in transformer where R_L is effectively isolated from the power supply V_{CC} using the transformer coupling as shown.

Push - Pull Amplifier



$$R_L' = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

Output load current = $k(i_{c1} - i_{c2})$

$= 2k(B_1 \cos \omega t + B_1 \cos 3\omega t + ...)$

Only odd harmonics are present. The push pull system has balanced out the even harmonics.

→ In class B operation, the operating point is at cut-off so that signal is amplified by one transistor only for one half of the cycle,

$$\eta = \frac{P_{ac \text{ to load}}}{P_{dc}} = \frac{\pi}{4}\left(\frac{V_{cc} - V_{min}}{V_{cc}}\right) \times 100$$

Theoretical max. η = max = $\pi/4 \times 100 = 78.5\%$

Also $\frac{P_{Dmax}}{P_{ac\,max}} = \frac{4}{\pi^2} = 0.4$

Under these maximum values of P_{ac} , P_D per transistor = 0.2 P_{ac} , P_D max = $\frac{1}{5}$ P_{ac} max

Maximum AC power obtained in class B push pull = 5 P_D (of the transistor).

Characteristic :

1. The ven harmonic are absent at the output of a push-pull amplifier i.e
   $I_C = 2I_1 \sin \omega t + 2 I_2 \sin 3\omega t + ...$
2. The amplifier gives more output power per transistor for a given amount of distortion.
3. Less distortion is achieved for a given power output per transistor.
4. The dc components of the output current of the two transistor oppose each other in the transformer. This eliminates the tendency of the output core of the transformer to saturate. Therefore, the losses in the transformer are minimized.
5. The effect of ripple voltage contained in the power supply are just balanced out since the current produced are in the opposite direction.
6. Due to non saturation of core the transformer contains less ferromagnetic material.
7. The output transformer for push pull amplifier circuit are lighter, smaller and less expensive than the transformer of comparable quality used in single ended transform amplifier.

Multistage Amplifier

Cascaded Amplifier

- Gain of one stage of amplifier may not be sufficient to obtain the required gain may be worked out in a single stage, the operating condition of the transistors may be impracticable.
- Overall gain is the product of gain of individual stages.
- $A_{VT} = A_{V1} \times A_{V2}$

Frequency Response of Cascaded Stages

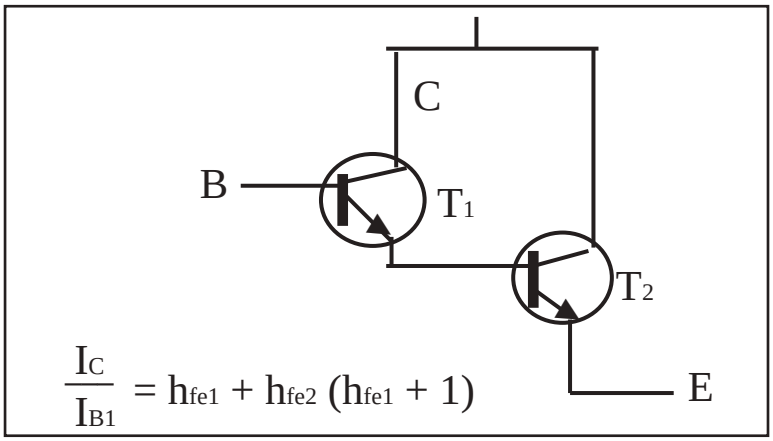
For n identical stages :

1. The upper cut-off frequency decreases
   $f_H = f_H \sqrt{(2^{1/n} - 1)}$
2. The lower cut off frequency increase
   $f_L = \frac{f_L}{\sqrt{2^{1/n} - 1}}$
3. Overall bandwidth decrease.
4. The gain bandwidth product remain constant.

5. The Transmission line parameter are used, i.e. A, B, C, D.

CC - CC (Darlington Pair)

The CC amplifier has high input impedance as a single transistor to increase the input impedance still further we use the Darlington emitter follower, which is CC-CC amplifier. The two transistors form a composite pair. this can be considered as single transistor with only three external lead.



$$\frac{I_C}{I_{B1}} = h_{fe1} + h_{fe2}\,(h_{fe1} + 1)$$

Assuming two transistor is having same h_{fe}

$$\frac{I_C}{I_{B1}} = h_{fe} \times h_{fe} = h^2_{fe} \quad ; \quad A_v \cong 1$$

Input Impedance

$R_i = h_{ie1} + (h_{fe1} + 1)\, h_{ie2}$

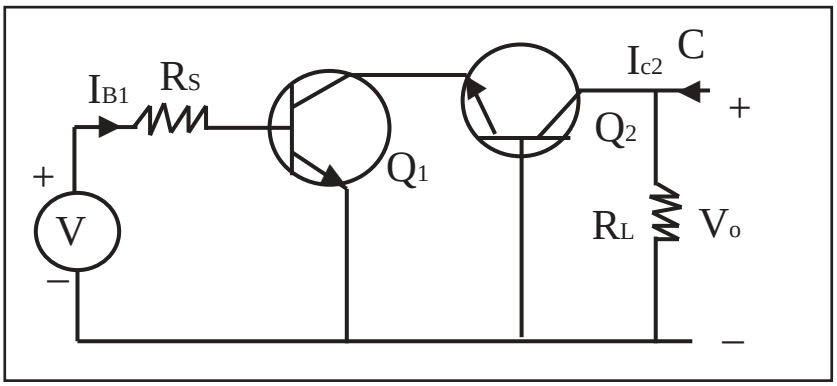
$R_i = 2h_{ie2}\,(h_{fe1} + 1)$

Assuming $h_{ie1} = h_{ie2} = h_{ie}$

Cascode Connection

This CE - CB connection

- Common emitter stage drives a common base amplifier.
- Gain can be improved by using large value of R_L over a wide range of frequencies.



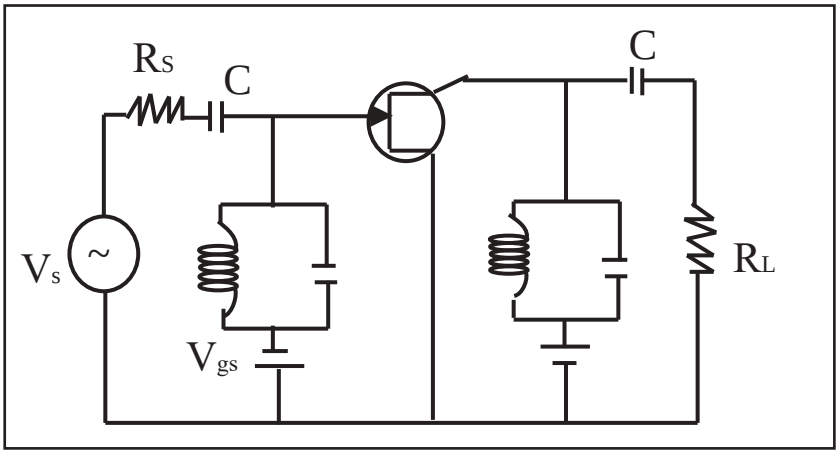
- Overall current gain $A_I = \frac{I_{C2}}{I_{B2}} = \beta_0$
- Voltage gain = $A_v = \frac{-\beta_0 R_L}{(R_s + r_{be})}$
- Output resistance of a CB stage is high, so we can connect a large load resistance R_L.
- This input resistance for the CB stage is low and this is the load resistance for the CE stage. The low input resistance of CB stage makes Q_1 operate into a short-circuit load, so voltage gain of common emitters stage is low. This cause reduces the input capacities so its Bandwidth gets increased.
- It is used in wide Band amplifiers due to its large bandwidth.

Tuned Amplifier

To provide gain at particular frequency tuned circuit are used at the input and output terminal. It is operated on RF frequency. The effective Q of the resonant circuit be high enough so the V_o consist only the direct voltage and fundamental component of signal i.e. of to eliminate the harmonics.

Function of the resonant circuit are :

1. To provide the correct load impedance.
2. To reject the unwanted harmonic.
3. To couple the power to the load.



Differential Amplifier

It is the basic building block of the operational amplifier :

- The first stage of an op-amp is Differential amplifier (DA).
- DA consists of two transistor which are emitter coupled and whole characteristic are identical.

There are two type of input signal to the DA :

Differential mode : $V_d = V_1 - V_2$

Common mode : It is the average between the input voltage V_2 and V_1

$$V_c = \frac{V_1 + V_2}{2}$$

High frequency Analysis

$$A_{DM} = \frac{-h_{fe} \cdot R_L}{R_s + r_{b'b} + r_{b'e}} = \frac{-h_{fe} \cdot R_L}{r_{b'e}} = -g_m R_L$$

$$A_{CM} = \frac{-g_m \cdot R_L}{1 + 2\, g_m R_E}$$

Low frequency analysis

$$A_d = \frac{-h_{fe} \cdot R_o R_L}{h_{ie} (R_o + 2R_L)}$$

$$A_c = \frac{-h_{fe} \cdot R_L}{h_{ie} + 2(1 + h_{fe})R_e}$$

Where ADM and ACM is known as differential mode gain and common mode gain.

Common mode rejection ration (CMRR)

- $CMRR = \frac{A_{DM}}{A_{CM}}$
- $CMRR = 1 + 2g_m R_E \approx 2\, g_m \cdot R_E$
- For large value of CMRR, we need large value of R_E, so use current source having high output resistance for FET based differential amplifiers.
- $CMRR = \frac{1 + 2\, R_s \mu}{r_d} \approx 2g_m R_s$

Feedback Amplifier Topologies

There are four basic type :

1. Shunt-Shunt
2. Shunt-Series
3. Series-Shunt
4. Series-Series

These designation corresponds to the input and output port connection respectively between the feedback network and the basic amplifier.

Gain with feedback

$$A_f = \frac{X_o}{X_s} = \frac{A}{1 - \beta . A}$$

Where A = transfer function without feedback.

If $| A_f | < | A |$, the feedback is termed as negative.

And if $| A_f | > | A |$, the feedback is termed as positive.

Fundamental Assumption

Three conditions are implicit in the representation of the ideal feedback amplifier.

1. The input signal is transmitted to the output through the amplifier A and not through the feedback networ β. Means feedback network is unilateral.
2. The feedback signal is transmitted from output to input through the feedback network only.
3. The transfer ratio β is independent of source and load resistance.

Property of Negative-Feedback Amplifiers

Although negative feedback results in reduced gain, it is used because of following reasons :

- Bandwidth get increased.
- Effect of noise get reduced
- Distortion get reduced.

Input Impedance in Feedback Amplifier Input Resistance

If the feedback signal is returned to the input in series with the applied voltage, the input impedance get increased.

$$R_{if} = R_i (1 - \beta A)$$

Where, R_{if} = Input resistance after feedback

R_i = Input resistance without feedback.

- For negative feedback V_f is 180º out of phase with V_s,V_i is less than it would be if V_f were absent. Hence $I = V_i / R_i$ decreased.
  Causes the ratio V_s / I to increase.
- If shunt connection is used at the input of a negative feedback amplifier, the impedance decreases.

$$R_{if} = \frac{R_i}{(1 - \beta \, . \, A)}$$

Output Impedance

When the output of a feedback employs a shunt connection, negative feedback reduces the Output resistance .

$$R_{of} = \frac{R_o}{(1 - \beta \, . \, A)}$$

Output impedances increased when a negative feedback amplifier employs a series connected output.

$R_{Of} = R_o (1 - \beta.A)$

Effect of feedback on Bandwidth

Open loop gain $A_{OL} = \dfrac{A_o}{\left[1 + \left(\dfrac{S}{\omega_n}\right)\right]}$ (without feedback)

Return Ratio

$$T(s) = \frac{T_o}{\left[1 + \left(\frac{S}{\omega_n}\right)\right]}$$

Where A_o and T_o are the midband value of A_{OL} and T(s), ω_n is angular frequency of the dominant pole.

$$A(s) = \frac{A_{OL}}{1 + A_{OL} \cdot T(s)} = \frac{A_{FO}}{\left[1 + \left(\frac{S}{\omega_n}\right)\right]}$$

where, $A_{FO} = \frac{A}{(1 + T_o)}$

$\omega_H = (1 + T_o)\, \omega_n$

Negative feedback has increased the bandwidth by a factor $(1 + T_o)$, the same factor by which A_{OL} is reduced.

Stability

In the design of a feedback amplifier, it must be ascertained that the circuit is stable at all frequencies.

A system is stable if and only if all bounded input signal produce bounded output signals

- If a pole of transfer function exists with a positive real part, this cause output to increase exponentially with time and hence unbounded.

Stability of Feedback Amplifiers

$$A_i(s) = \frac{A_{OL}(s)}{1 + T(s)}$$

Amplifier without feedback is stable if all the pole of A_{OL} lie in the left half of s-plane.

Amplifier with feedback is stable if all the zero of T(s) lie in the left half of s-plane.

Feedback Amplifier Configuration

Feedback is the process whereby a portion of the output is returned to the input to form part of the system excitation.

Feedback was used to make the operating point of a transistor insensitive to both manufacturing variation in β_1 and temperature.

Effect of negative feedback on amplifier characteristic

	Type of feedback			
	Volatage series	Current series	Current shunt	Volatge shunt
Z_{out}	Decrease	Increases	Increases	Decreases
Z_{in}	Increases	Increases	Decreases	Decreases
Improves characteristics of	Volatge Amplifier	Transconduct--ance amplifier	Current Amplifier	Trans-Resistance amplifier
Desensitizes	A_{vf}	G_{Mf}	A_{if}	R_{MI}

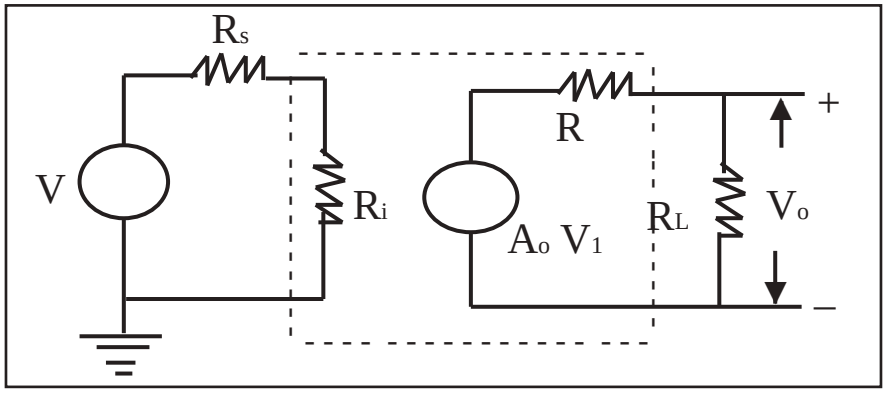
Type of Feedback Amplifiers

Voltage Amplifier Or Voltage Series Amplifier

$R_i >> R_s$; $R_o << R_L$

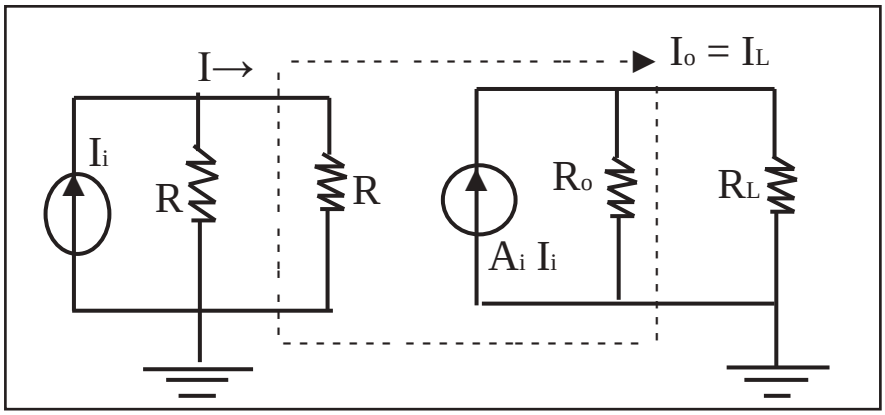
R_i = Input resistance of the amplifier

This circuit provides an output voltage proportional to the input voltage. $R_i >> R_s$ and $R_o >> R_L$.



The current Amplifier or Current Shunt Amplifier

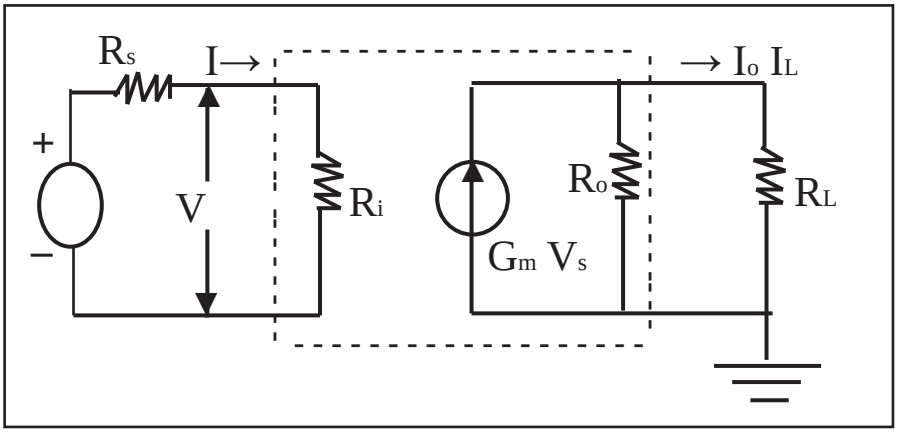
An ideal current-controlled source has zero input resistance R_i and has infinite output resistance R_o.



$|R_i| << R_s$ and $|R_o| >> R_L$; $I_o = A_i I_i$

Output current is proportional to input current.

The Voltage-Current Converter or trans-conductance Amplifier (Voltage Controlled current source) or Current Series Amplifie

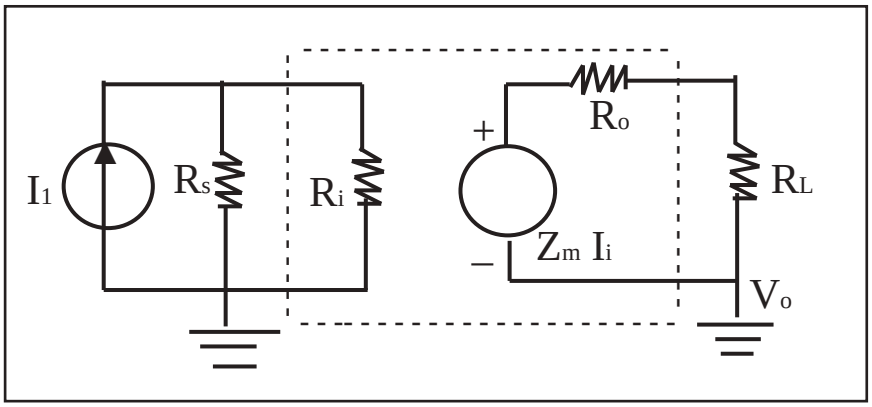


This ideal voltage - controlled current source.

$|R_i| >> R_s$ and $|R_o| >> R_L$

$I_o = G_m V_s$

Current-voltage Converter or Trans-Impedance Amplifier or Voltage Shunt Amplifier (Current Controlled Voltage Source)



This is ideal current controlled voltage source

$R_i >> R_s$ and $|R_o| << R_L$

$V_o = Z_m I_s$

Operational Amplifier

1st Stage : Difference amplifier

2nd Stage : High gain linear amplifier

3rd Stage : Emitter follower.

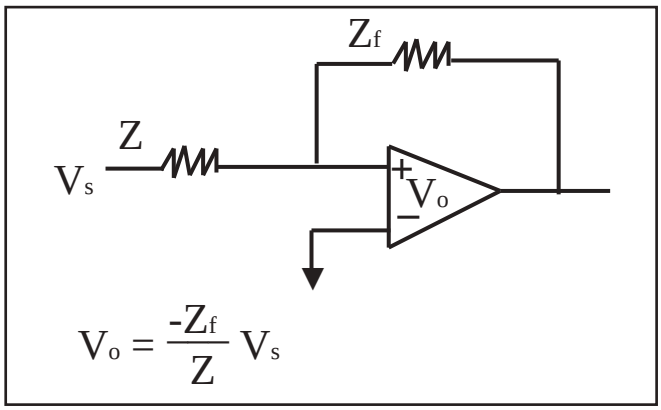
4th Stage : DC level shifter and output amplifier

Ideal Op-amp Characteristics

1. Input resistance is infinite, $Z_{in=\infty}$, so no current enters the input terminal.
2. A zero output resistance, $Z_{out} = 0$
3. Infinite voltage gain, $A_v = \infty$
4. Characteristics do not drift with temperature.

Application of OPS Amplifier

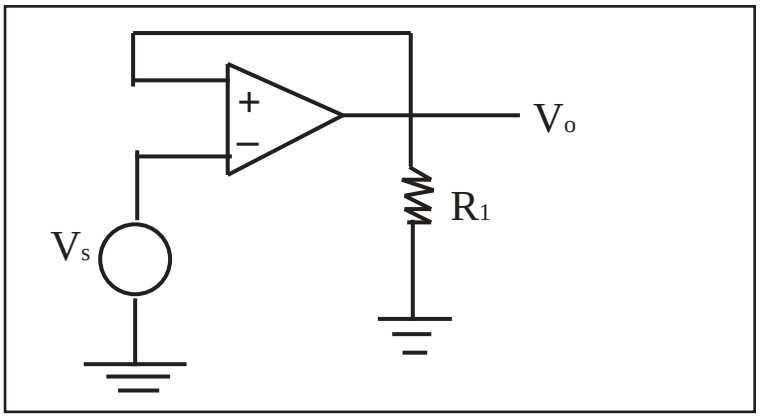
Inverting Amplifier



$$V_o = \frac{-Z_f}{Z} V_s$$

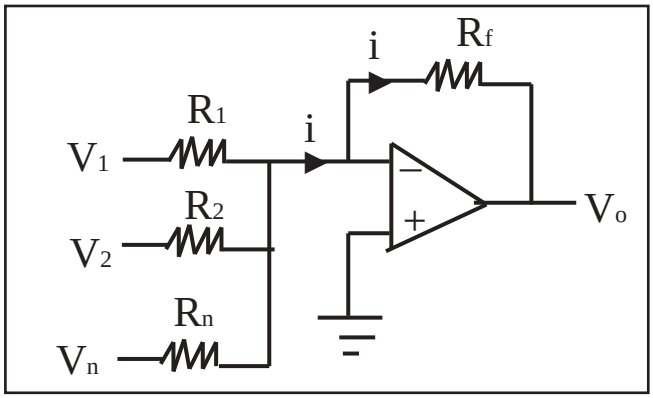
Input Impedance : The input resistance is equal to resistance Z.

Unity Follower



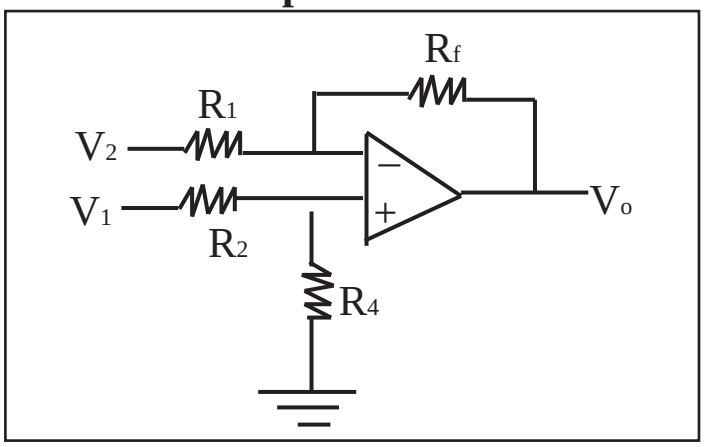
The output signal is in phase with the input signal and of same magnitude. Input impedance is very high, so it provides very good isolation between stages.

Summing Amplifier



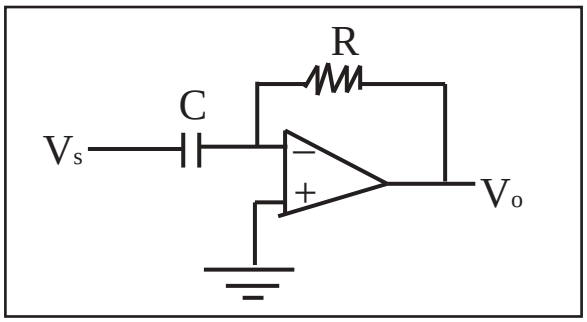
$$V_o = -\left(\frac{R_f V_1}{R_1} + \frac{R_f V_2}{R_2} + \frac{R_f V_n}{R_n}\right)$$

Differential Amplifier



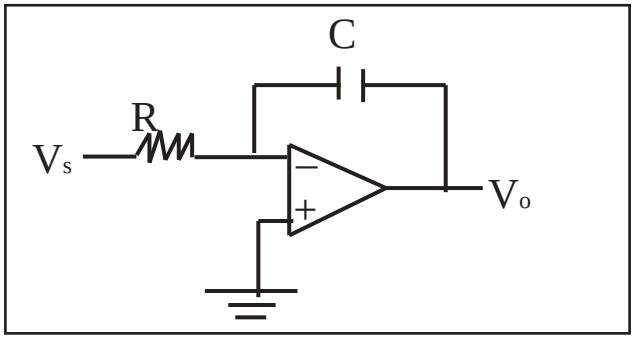
If $\frac{R_2}{R_1} = \frac{R_4}{R_3}$; $V_o = \frac{R_f}{R_1}[V_1 - V_2]$

Differentiator



$$\frac{V_o(s)}{V_s(s)} = -sRC$$

Integrator



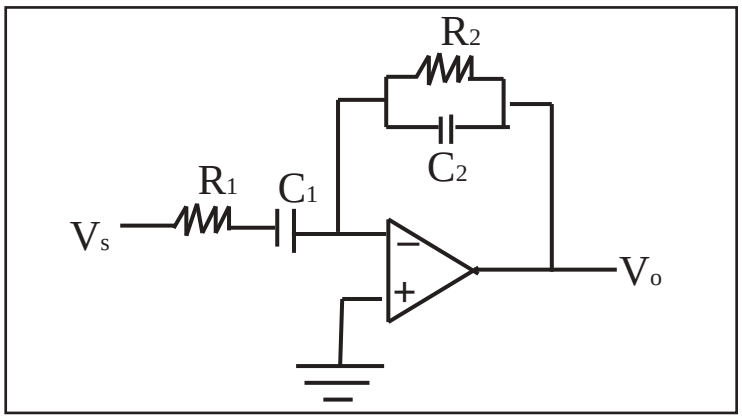
$$\frac{V_o(s)}{V_s(s)} = \frac{1}{sRC}$$

All Pass Filter

$$\frac{V_o}{V_i} = \frac{1 - j\omega RC}{1 + j\omega RC} = \frac{1 - sRC}{1 + sRC}$$

$|H(j\omega)| = 1$ and phase shift $= 2\tan^{-1}(\omega RC)$

Band Pass Filter



$$\frac{V_o}{V_s} = \frac{-sC_1 R_2}{(1 + sC_2 R_2)(1 + sC_1 R_1)}$$

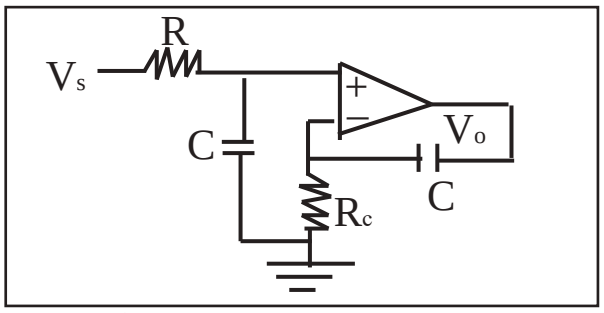
Type of Filter

Putting $\omega = 0$ (capacitor open-circuit) and

$\omega = \infty$ (capacitor short-circuited)

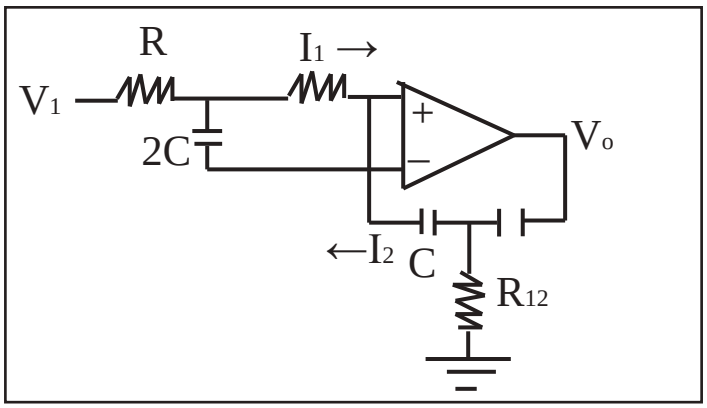
In above circuit when $\omega = 0$, C_1 = open circuit and $V_o = 0V$, similar for $\omega = \infty$ ($C_1 = C_2$) so it does not pass high as well as low frequency so it is band pass.

Non-Inverting Integration



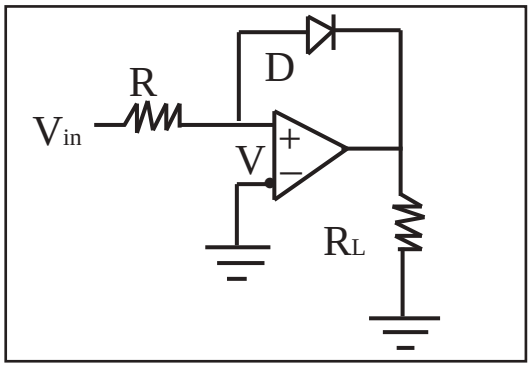
$$V_o = \frac{1}{RC}\int V_s \, dt$$

Double Integration



$$\frac{V_o}{V_s} = -\frac{1}{(sRC)^2}$$

Logarithmic Amplifier



When $V_{in} < 0$; diode is off, Op-amp behaves as comparator. At this time

$V_o = + V_{sat}$

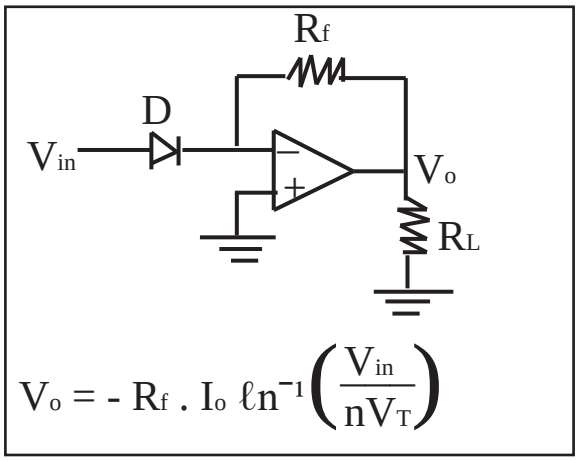
- When $V_{in} > 0$ diode is ON

  $V_o = - 0.7$ V

- For small range V_{in} . It behaves as logrithmic amplifier

$$V_o = 2.3 \frac{KT}{q} \log_{10}\left(\frac{V_{in}}{R_L I_o}\right)$$

Antilogrithmic Amplifier



$$V_o = - R_f . I_o \ell n^{-1}\left(\frac{V_{in}}{nV_T}\right)$$

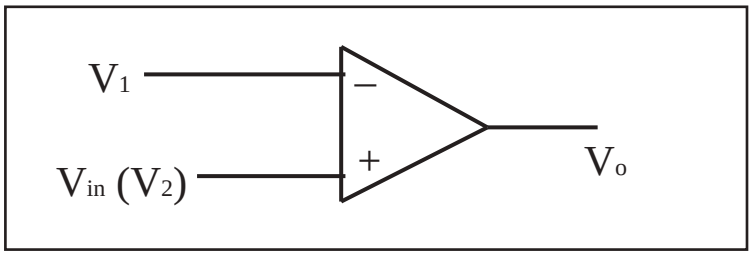
Comparator

In a comparator, the level of the applied input voltage is compared with a known reference voltage :

1. As a comparator, the level of the applied input voltage is compared with a known reference voltage.
2. As a comparator, the Op-amp are operated in the open loop condition without feedback resistor.
3. Since it is operated in open loop condition, the assumption ($V+ - V- = V_d = 0$) is not applicable.
4. Open loop gain is very high, so output goes to saturation levels ($\pm V_{cc}$)

even for very low inputs.

5. If 1 or 2V drops in R_c's of the transistor of the differential stage, the saturation voltage will be (± 13 V) for a supply voltage of (± 15 V).



If $(V_2 - V_1) = V_{in} > 0$, $V_o = + V_{sat}$

If $(V_2 - V_1) = V_{in} < 0$, $V_o = -V_{sat}$