DIGITAL ELECTRONICS

Digital Electronics : Combinational logic circuits, minimization of Boolean functions. IC families, TTL, MOS and CMOS. Arithmetic circuits, Comparators, Schmitt trigger, timers and mono-stable multi-vibrator. Sequential circuits, flip-flops, counters, shift registers. Multiplexer, S/H circuit. Analog-to-Digital and Digital-to-Analog converters. Basics of number system. Microprocessor applications, memory and input-output interfacing, Microcontrollers.

COMBINATIONAL LOGIC CIRCUITS

Digital circuit are divided into two broad categories.

1. Combinational circuit and
2. Sequential circuit.

Combinational Circuit.

The output at any instant of time depends upon the input present at the instant of time. No memory in these circuits.

Sequential Circuit

These are circuit in which the output at any time depends upon the present inputs as well as past input/outputs. Memory is essential for these type of circuit.

The Design Requirement of Combinational Circuit

* A set of statements * Boolean expression * Truth table

Following methods can be used to simplify the Boolean function :

1. Algebraic method
2. K-map technique
3. Variable entered mapping (VEM) technique and
4. Quine-Mc cluskey method.

MINIMIZATION OF BOOLEAN FUNCTIONS

Georga Boolean developed rules for manipulation of binary variable, known as Boolean algebra.

Table for Boolean

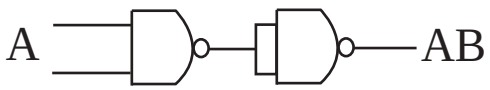
1.	$0.A = 0$	$A + O = A$
2.	$A.1 = A$	$A = 1 = 1$
3.	$A.A = A$	$A + A = A$
4.	$A.A' = 0$	$A + A' = 1$

Duality is defined for huntingtone system just as it is for other axiomatic system and the dual of a give expression can be derive for simply replacing the "." with "+" and "+" with "." and "." with 1's and 1's with 0's in the expression.

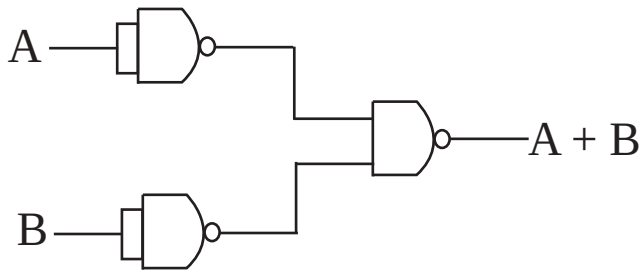
ALGEBRAIC THEOREMS

1. $A + AB = A$
2. $A + \overline{A}B = A + B$
3. $AB + A\overline{B} = A$
4. $AC + \overline{A}BC = AC + BC$
5. $AB + AC + \overline{B}C = AB + \overline{B}C$
6. $\overline{A.B.C} = \overline{A} + \overline{B} + \overline{C}$
7. $\overline{A + B + C} = \overline{A}.\overline{B}.\overline{C}$

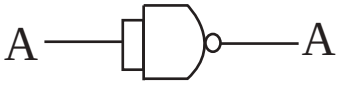
1. AND using NAND



2. OR using NAND

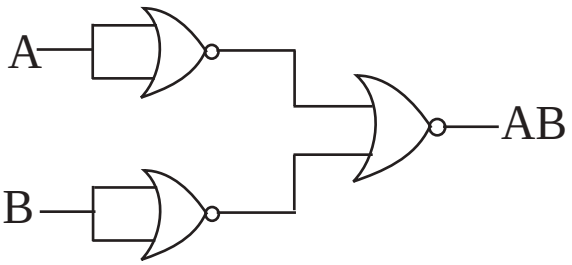


3. NOT using NAND

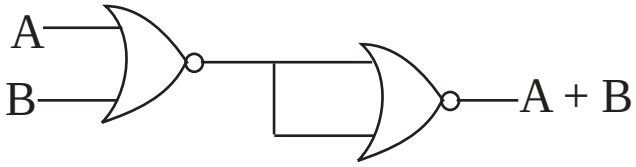


NOR = gate also used to find operation similar to that of AND. OR and NOT.

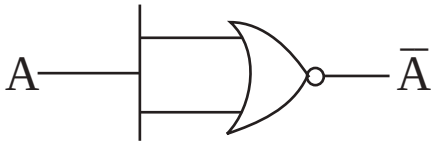
1. AND



2. OR



3. NOT



KARNAGUH MAP AND APPLICATIONS

Standard Representations for Logical Functions

Any arbitrary logic function can be expressed in the following forms.

Sum-of-product **(SOP),** and Product-of-sums form **(POS)**

Example : $Y = (A + BC)(B + \overline{AC}) = AB + BC + A\overline{C} = 0$

$= AB + BC + A\overline{C} = ABC + ABC + ABC + ABC + ABC$

$= ABC + AB\overline{C} + ABC + \overline{A}BC + A\overline{B}\overline{C}$

$= ABC + AB\overline{C} + \overline{A}BC + A\overline{B}\overline{C}$

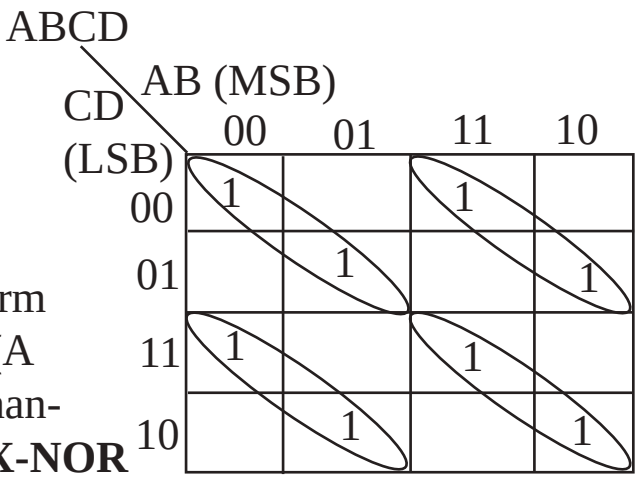
$Y = \Sigma 7, 6, 3, 4$

Note : If a logical function is specified in terms of minterm/max-term its maxterm minterm representation can be using this complementary property.

If $y = \Sigma m\,(0, 3, 5, 6, 9, 10, 12, 15)$

Then $\overline{y} = \pi m\,(1, 2, 4, 7, 8, 11, 13, 14)$

Some Special Cases of K-map



Making pair as shown. To write expression for the pair we follow this technique.

For first pair, we have two term 0000 and 0101. Now we see that (A and C) is same and (B and D) is changing like (00 to 11). This gives **EX-NOR** ($\odot$) type. If this case like (01 to 10) will give **EX-OR** ($\oplus$) operation. So,

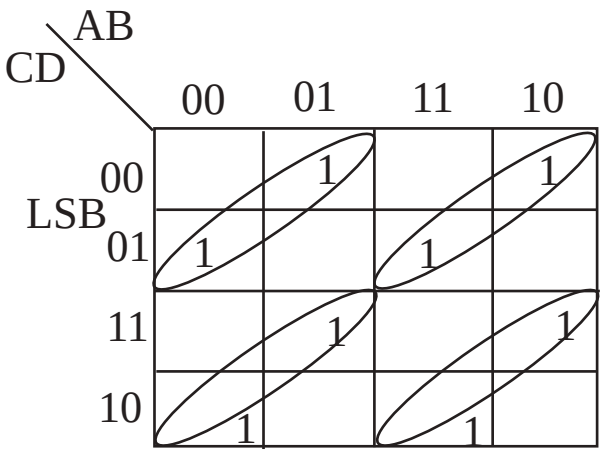
* 1st pair we can write $\overline{A}\,\overline{C}\,[B \odot D]$
* 2nd pair we have (1100 to 1001) = $A\overline{C}[B \oplus D]$ (as B and D change as 10 to 01)
* 3rd pair we have (0011 to 0110) = $\overline{A}\,C\,[B \oplus D]$
* 4th pair we have (1111 to 1010) = $AC[B \odot D]$

So, $Y = A\,C\,[B \odot D] + A\,C\,[B \oplus D] + AC\,[B \oplus D] + AC\,[B \odot D]$

$= (A\overline{C} + \overline{A}C)\,(B \oplus D) + (A\overline{C} + AC)\,(B \odot D)$

$= (A \oplus C)\,(B \oplus D) + (A \odot C)\,(B \odot D)$

Similarly we have



* 1st pair (0100 to 0001) = $\overline{A}\,\overline{C}\,[B \oplus D]$
* 2nd pair (1000 to 1101) = $A\,\overline{C}\,[B \odot D]$
* 3rd pair (0111 to 0010) = $\overline{A}C[B \odot D]$
* 4th pair (1011 to 1110) = $AC\,[B \oplus D]$

So, $Y = \overline{A}\,\overline{C}\,[B \odot D] + A\overline{C}\,[B \odot D] + \overline{A}C\,[B \odot D] + AC\,[B \oplus D]$

$= [AC + \overline{A}\overline{C}]\,[B \oplus D] + [A\overline{C} + \overline{A}C]\,[B \odot D]$

$= [A \odot C]\,[B \oplus D] + [A \oplus C]\,[B \odot D]$

IC FAMILIES (TTL MOS AND CMOS)

BIPOLAR LOGIC FAMILIES.

* Main elements of a bipolar IC (integrated circuit) are resistors, diodes (which are also capacitors) and transistors.
* Two types of operations in Bipolar IC's :
  1. Saturated 2. Non-Saturated

1. In saturated logic the transitors in the IC are driven to saturation so its operation is slow due to charge storage problem.
2. In Non saturated case the transistors are not driven into saturation so its operation is fast.

THE SATURATED BIPOLAR LOGIC FAMILIES ARE

1. Resistor-transistor logic (RTL)
2. Direct-couple transistor logic (DCTL)
3. Integrated-injected logic (I^2L)
4. Diode-transistor logic (DTL)
5. High threshold logic (HTL)
6. Transistor-transistor logic (TTL)

The Non-Saturated Bipolar Logic Families

1. Schottky TTL 2. Emitter-coupled logic (ECL)

Unipolar Logic Families

MOS devices are unipolar devices and only Enhancement MOSFET's are employed in MOS logic circuit.

1. PMOS 2. NMOS and
3. CMOS (complementary MOS)

* PMOS uses only p-channel MOSFET's
* NMOS uses only n-channel MOSFET's
* CMOS uses both n and p channel MOSFET's fabricated on the same silicon chip.

IC classification	Equivalent individual	Numbers of components
SSI	Less than 12	Up to 99
MSI	12 - 99	100 - 999
LSI	100 - 999	1000 - 9999
VLSI	1000 - 9999	10,000 - 99,9999
ULSI	10,000 or more	100,000 and above

VARIOUS CHARACTERISTICS

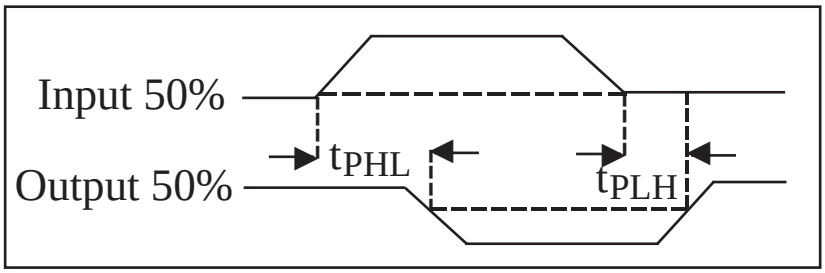
Various characteristics of digital IC's are used to compare their performance are:

1. Speed of operation
2. Power dissipation
3. Figure of Merit
4. Fanout
5. Current and voltage parameters
6. Noise immunity
7. Operating temperature range
8. Power supply requirements
9. Flexibility available
10. Digital signal voltage level

Speed of Operation

The speed of a digital circuit is specified in term of the propagation delay times. The input and output waveforms of a logic gate is shown below:

The delay times are measured between the 50% voltage levels of input waveform and output waveform.



There are two Delay Time

t_{PHL} when the output goes from High to Low state

t_{PLH} when the output waveform goes low to high.

The propagation delay time of the logic gate is taken as the average of these two delay times.

Power Dissipation

This is the amount of power dissipated in an IC. It is determined by the current I_{cc}, that it draws from the V_{cc} supply, and is given by $V_{cc,X}$ where I_{cc} . I_{cc} is the average value of I_{cc} (0) and I_{cc} (1).

Digital Electronics

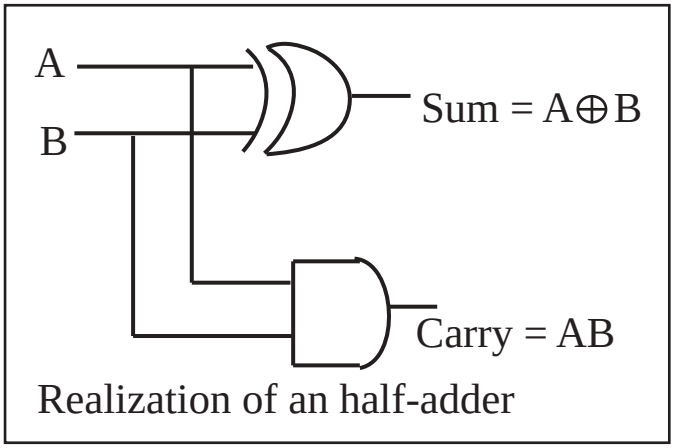
Arithmetic Circuit

Half Adder :

A logic circuit for the addition of two one-bit number is referred to as an half-adder.

$S = A \oplus B$

$C = AB$



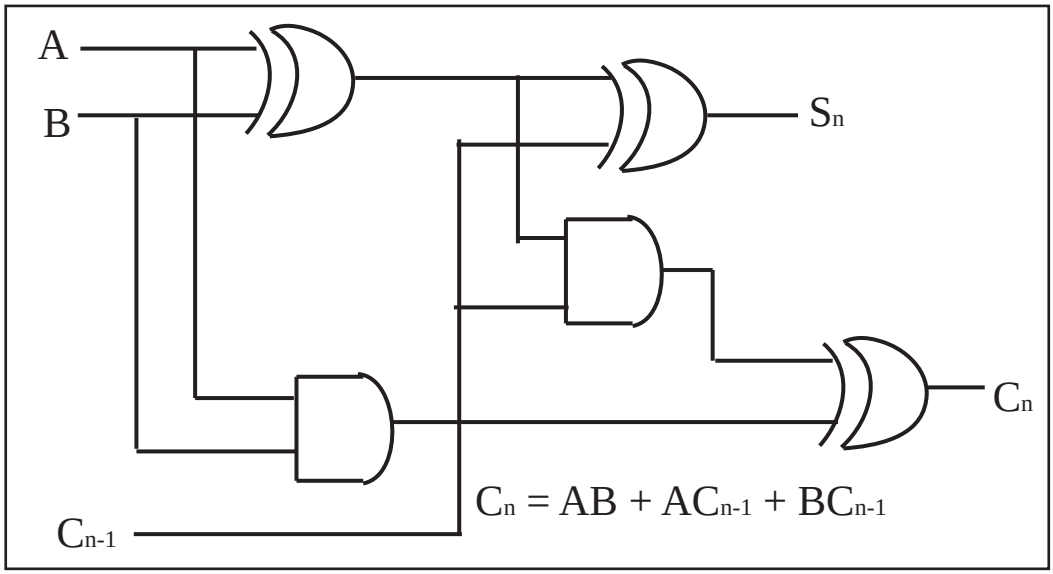
Realization of an half-adder

Full Adder

An half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multibit addition is performed. For this purpose an extra (third) input is added and this circuit is used to add A_n , B_n and C_{n-1} .

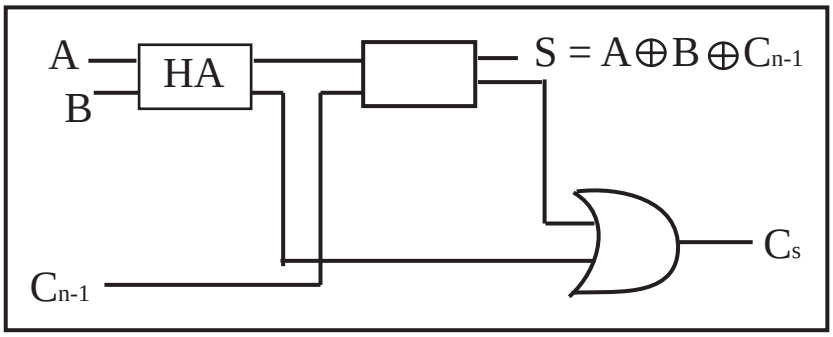
We have $S_n = A_n \oplus B_n \oplus C_{n-1}$

$C_n = A_n B_n + B_n C_{n-1} + A_n C_{n-1}$

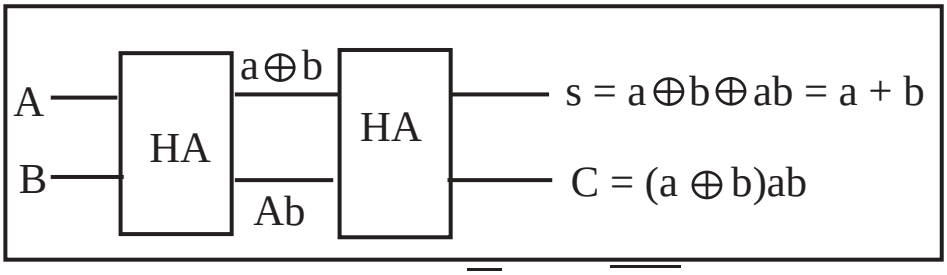


Realization of Full Adder using HA And OR gate

Full adder can be realized with two half adder (HA) and OR gate.



OR gate also be realized by cascading two HA as shown below :



$S = (a \oplus b) \oplus ab = (a \oplus b)\overline{ab} + ab(\overline{a \oplus b})$

$= (a \oplus b)(\bar{a} + \bar{b}) + (ab)(\bar{a} \cdot \bar{b} + ab)$

$= (a\bar{b} + \bar{a}b)(\bar{a} + \bar{b}) + a\,b = a\bar{b} + \bar{a}\,b + a\,b$

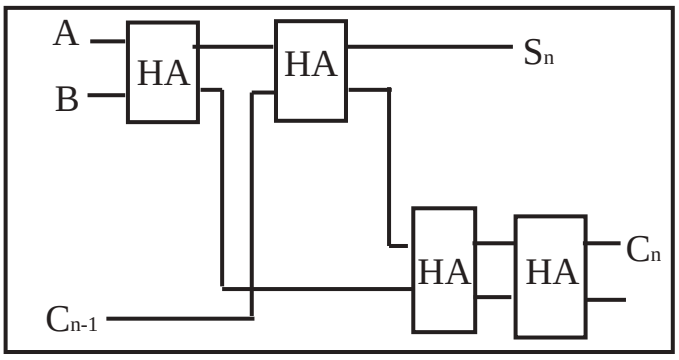
$= (a\bar{b} + \bar{a}b) + ab = a[\bar{b} + b] + \bar{a}b = a + \bar{a}b$

$= a + b$; $C = (a \oplus b)ab = 0$

So S (output) of final HA = (a + b)

So Cascaded HA behaves as OR gate

So realization of Full adder only with using HA

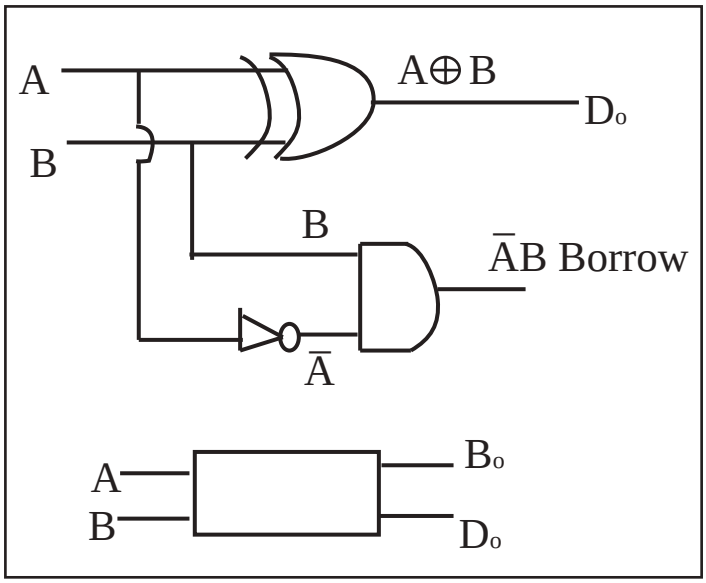


Half Subtractor

(A - B) two bit subtractor

Truth Table

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0
		$A \oplus B = \bar{A}B + \bar{B}A$	$\bar{A}B$



Binary To Gray Code Converter

Suppose B_o, B_1, B_2, B_3 (are four bit) input in Binary form and G_o, G_1, G_2, G_3 (output in Gray Code)

So we have

$G_3 = B_3$

$G_2 = B_2 \oplus B_3$

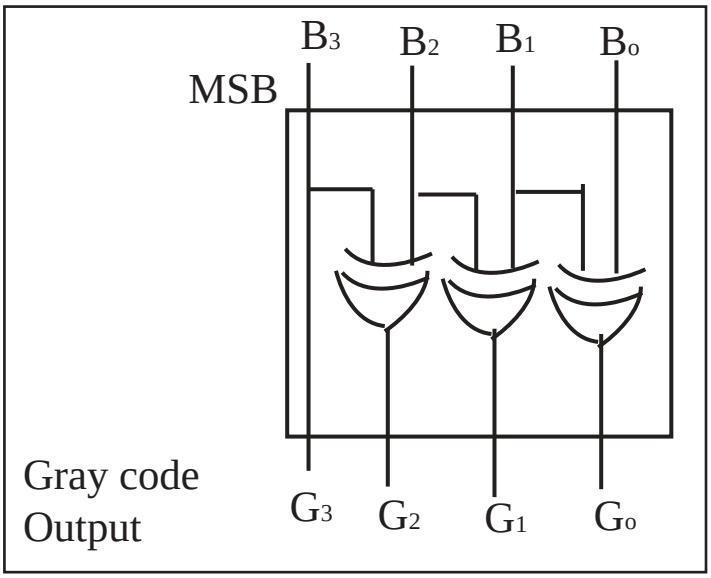
$G_1 = B_1 \oplus B_2$

$G_o = B_o \oplus B_1$

Example : Binary Input : 1 0 0 0 1 0

Gray : 1 1 0 0 1 1

i.e MSB remain same and rest of bit is obtain by EX-OR or previous and current bit.



Gray-To-Binary Code Converter

Gray code input (G_3 G_2 G_1 G_o)

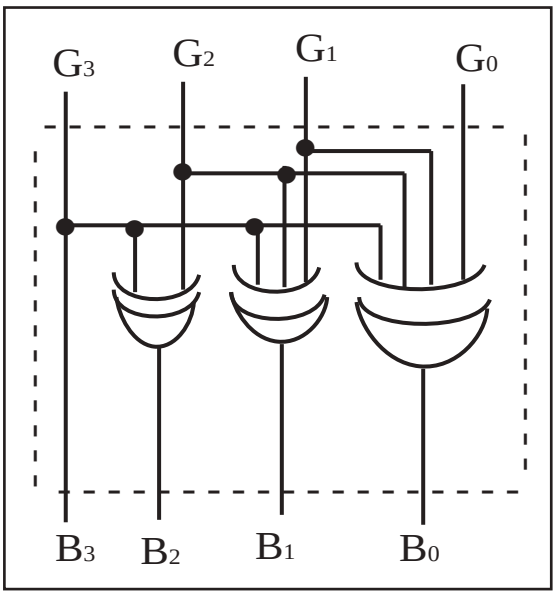
Binary output ($B_3\ B_2\ B_1\ B_0$)

$B_3 = G_3$

$B_2 = G_2 \oplus G_3$

$B_1 = G_1 \oplus G_2 \oplus G_3$

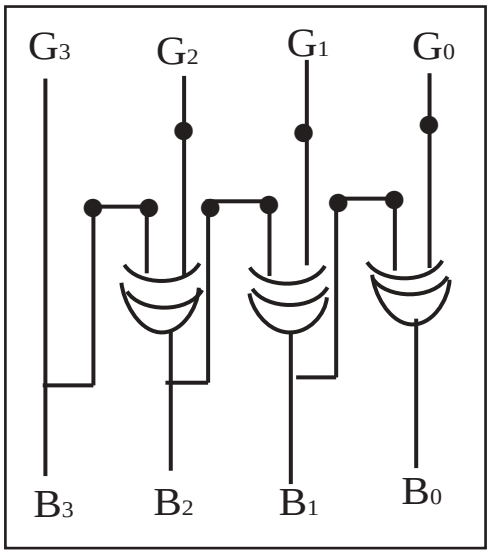
$B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3$



Example :

Gray code :	1	1	0	0	1	1
Binary code :	1	0	0	0	1	0

Error Detecting Code



COMPARATORS :

One Bit Comparator

Suppose you have two, one bit number A and B

A > B only if A = 1 and B = 0 i.e $C = A\overline{B} = 1$

A < B only if A = 0 and B = 1 i.e. D = $\bar{A}B = 1$

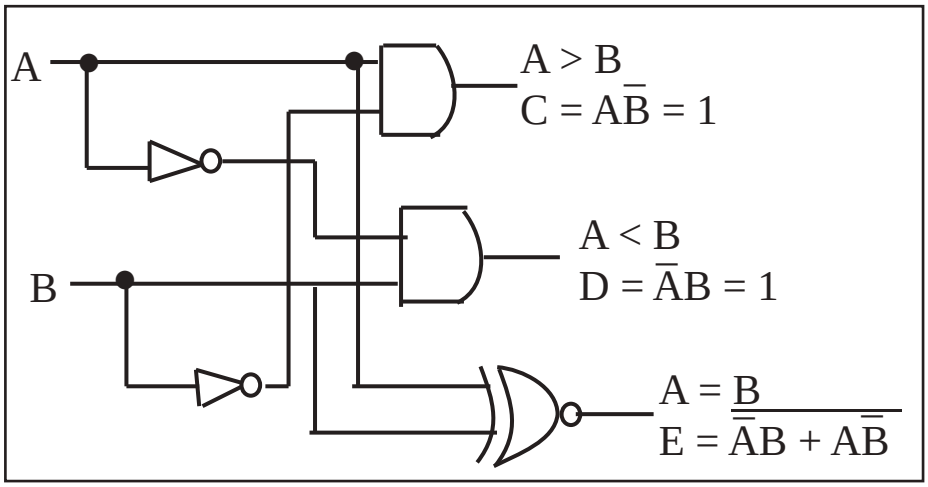
A = B if (A = 1 and B = 1) or (A = 0 and B = 0)

So,

A > B should givehigh signal when $A\bar{B}$ is high

A < B should give high signal when $\bar{A}B$ is high

A = B should give high signal when $\overline{\bar{A}B + A\bar{B}}$ is high



FOUR BIT COMPARATOR

$A = A_3\ A_2\ A_1\ A_0$

$B = B_3\ B_2\ B_1\ B_0$

For A > B

$C = A_3\bar{B}_3 + E_3A_2\bar{B}_2 + E_3E_2\ A_1\bar{B}_1 + E_3E_2E_1\ A_0\bar{B}_0$

For A < B

$D = \bar{A}_3B_3 + E_3\bar{A}_2B_2 + E_3E_2\ \bar{A}_1B_1 + E_3E_2E_1\ \bar{A}_0B_0$

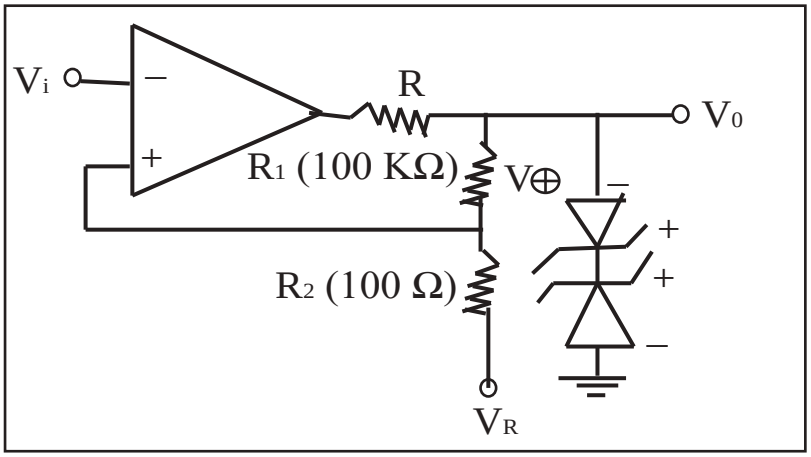
For A = B

$E = \overline{E_3E_2E_1E_0}$

where, $E_n = A_n\ \bar{B}_n + \bar{A}_n\ B_n$

SCHMITT TRIGGER

Regenerative Comparator (Schmitt Trigger)



R : Used for current limiting.

Output voltage is referred by using two zener diode Back to back.

$V_o = (V_z + V_D)$ for $V \oplus V_i$

$V_o = (V_z + V_D)$ for $V \oplus V_i$

where, V_z = Zener breakdown voltage

V_D = Diode cut in voltage

$$V\oplus = \frac{R_2}{R_1 + R_2} \cdot V_o + \frac{R_1 V_R}{R_1 + R_2}$$

where, $V\oplus > V_1$, $V_o = +(V_z + V_D)$

At the point where $V_1 = V\oplus = V_1$

$$V_1 = \frac{R_2}{R_1 + R_2} \cdot V_o = \frac{V_R R_1}{R_1 + R_2} \qquad (1)$$

After $V_1 > V_2$, output V_o switches to $-(V_z + V_D)$

So we have

$$V_2 = \frac{R_2}{R_1 + R_2} \cdot V_o = \frac{V_R R_1}{R_1 + R_2} \qquad (2)$$

From (1) and (2) we can see that

$V_2 < V_1$

Conclusion

For increasing value of V_i output switches from V_0 to $-V_0$ after $V_i > V_1$ and it will continue to be same when V_i is decreasing then output changes from $-V_0$ V_0 at the value of V_2 which is less than that of V_1. Due to the difference in V_1 and V_2 , switching point, we referred this situation as hysteresis voltage.

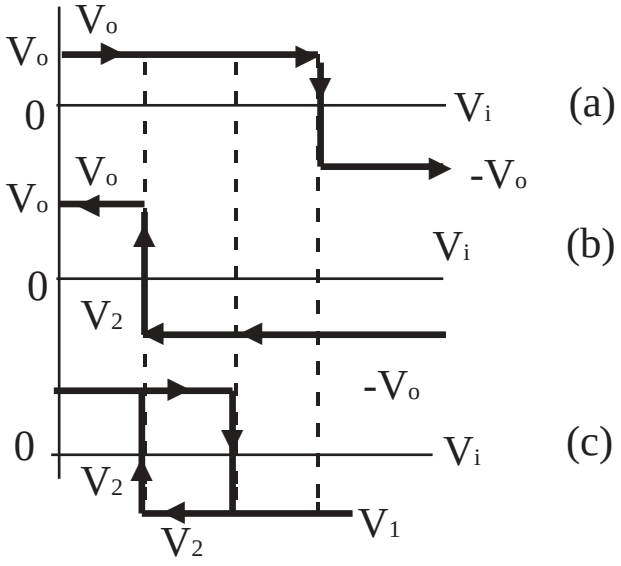


Figure : A Schmitt trigger, The transfer characteristics for (a) Increasing V_i and (b) Decreasing V_i (c) The compective input output curve.

Timers And Mono Stable Multi Vibrator

Timing Circuit

Digit system require some kind of a timing waveform for example, a source of trigger pulses, for clocked sequential systems. rectangular waveform is most desirable. The generators of rectangular waveforms are referred to as multivibrators.

Three Types of Multivibrator

1. Astable (or free running) multivibrator.
2. Monostable multivibrator (one-shot), and
3. Bistable multivibrator (or flip-flop).

1. Astable multivibrator is nothing but an oscillator, which generates rectangular waveform. It has two quasi-stable states, and doesnot require any triggering; hence it is referred to as a **free running** multivibrator.

2. Monostable Multivibrator has one stable state i.e under steady state condition, its output is fixed it is either in the low or the high state. When the circuit is triggered with an externally applied pulse it goes into the other state, i.e if it was in low state, it will go to high and vice-versa. The circuit remains in this state for the elements used in the circuit.

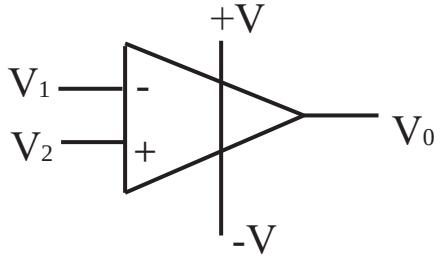
3. Bistable Multivibrator : A multivibrator circuit in which both the states are stable is referred to as a bistable multivibrator or FF. The circuit makes transition pulse is applied.

OP-AMP and its Application in Timing Circuit

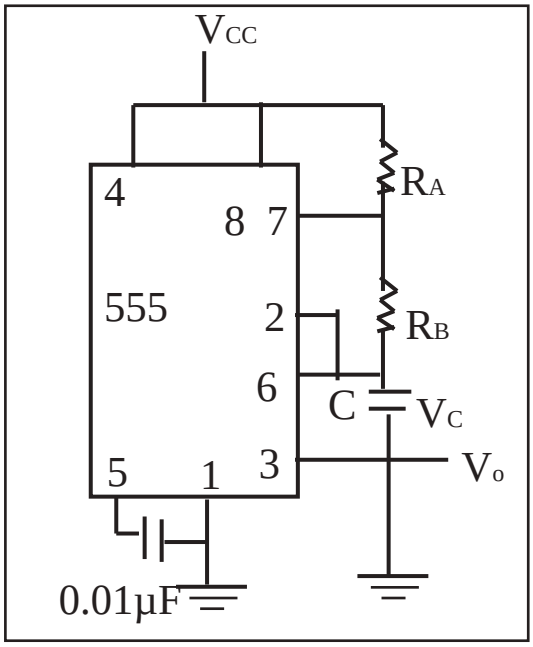
We know property of OP-AMP

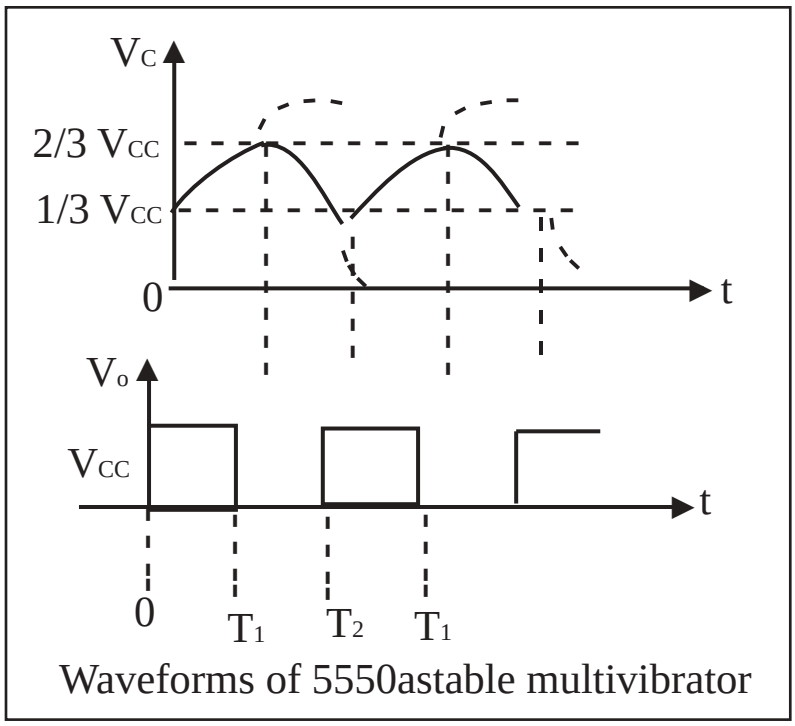
- Very high gain
- High Input impedance
- Low output impedance

Block Diagram of OP-AMP



Astable Multivibrator





Waveforms of 5550astable multivibrator

$T_1 = 0.7C [R_A + R_B]$

$T_2 = 0.7C R_B$; $T = 0.7C [R_A + 2R_B]$

Sequential Circuits

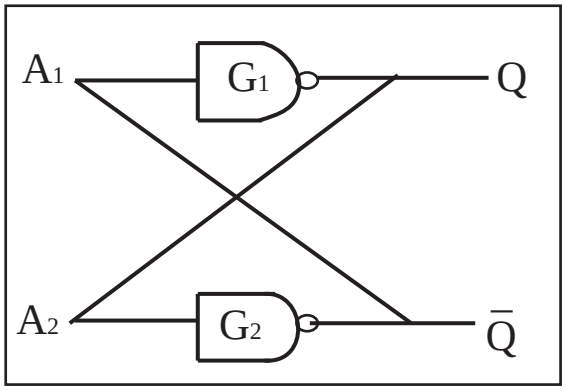
Consists of combinational circuit, which accept digital signals from external inputs and output of memory elements.

Flip Flops

A 1-bit Memory Cell

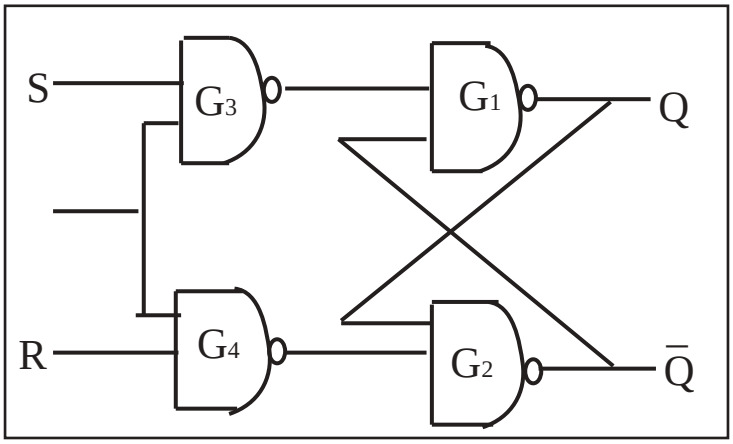
The basic digital memory circuit is known as flip-flop. It has two stable, 1 state and 0 stste

It consists of two inverters G_1 and G_2 (NAND gates based).



- The output Q and $\bar{Q}$ are complementary.
- The circuits has two states, in one of the stable stste Q = 1 which is known as (Set state), where as in the other hand, other stable Q = 0 known as (reset state).
- If the circuit is in state 1, it continues to remain in this state and similarly if it is in 0 stste. This property is known as memory, it can store 1-bit of digital information.
- This circuit is alos known as **latch**.

Clocked S-R Flip-Flop



Truth Table of S-R Flip-Flop

Inputs		Output
S_n	R_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	NA/Prohibit

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
	0	1	0
	1	0	1 ←
	1	1	?
1	0	0	1 ←
	0	1	0
	1	0	1 ←
	1	1	?

$$Q_{n+1} = \overline{Q}_n S_n \overline{R}_n + Q_n \overline{S}_n \overline{R}_n + Q_n S_n \overline{R}_n$$

	$\overline{S}_n \overline{R}_n$	$S_n \overline{R}_n$	$S_n R_n$	$\overline{S}_n R_n$
$\overline{Q}_n$		1		
Q_n	1	1		

$$Q_{n+1} = S_n \overline{R}_n + \overline{R}_n Q_n$$

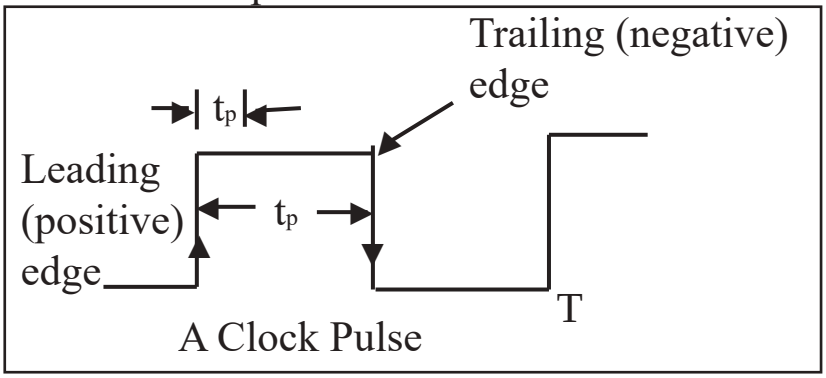
Excitation Table for S-R

Q_n	Q_{n+1}	S_n	R_n
0	0	0	ϕ
0	1	1	0
1	0	0	1
1	1	ϕ	0

Where, ϕ = (don't care)

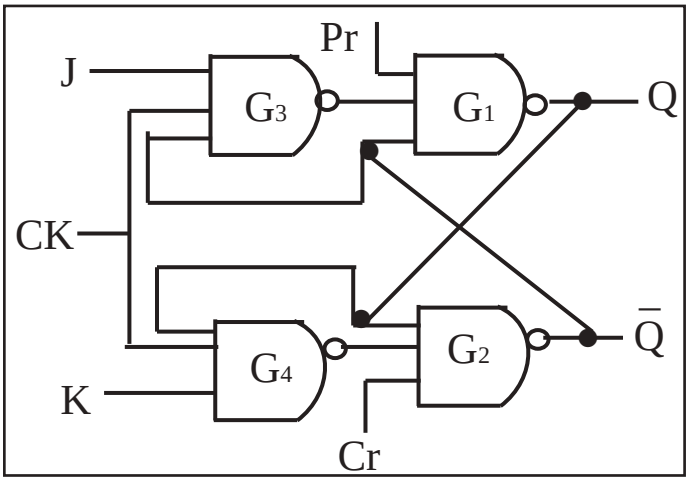
The Race-Around Condition

The difficulty of both input 1 (S = R = 1) being not allowed in an S-R flip flop is eliminated in J-K flip flop by using the feedback connection from outputs to the input of the gates. When J = K = 1 and Q = 0 and a pulse as shown is applied at the clock input.



J-K Flip Flop

J-K FF is called a **universal flip flop** because the other FF, like D, S-R, T can be derived from it. It is a versatile device.



Pr = Present

Clr = Clear (are asynchronous input)

Truth Table for JK

Inputs		Outputs
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

State Table for JK

Q_n	J_n	K_n	Q_{n+1}
0	0	0	0
	0	1	0
	1	0	1 ←
	1	1	1 ←
1	0	0	1 ←
	0	1	0
	1	0	1 ←
	1	1	0

$Q_{n+1} = \bar{Q}_n J_n \bar{R}_n + \bar{Q}_n J_n K_n + Q_n \bar{J}_n \bar{K}_n + Q_n J_n \bar{K}_n$

	$\bar{J}_n \bar{K}_n$	$\bar{J}_n K_n$	$J_n K_n$	$J_n \bar{K}_n$
Q_n			1	1
Q_n	1			1

$Q_{n+1} = J_n \bar{Q}_n + \bar{K}_n Q_n$

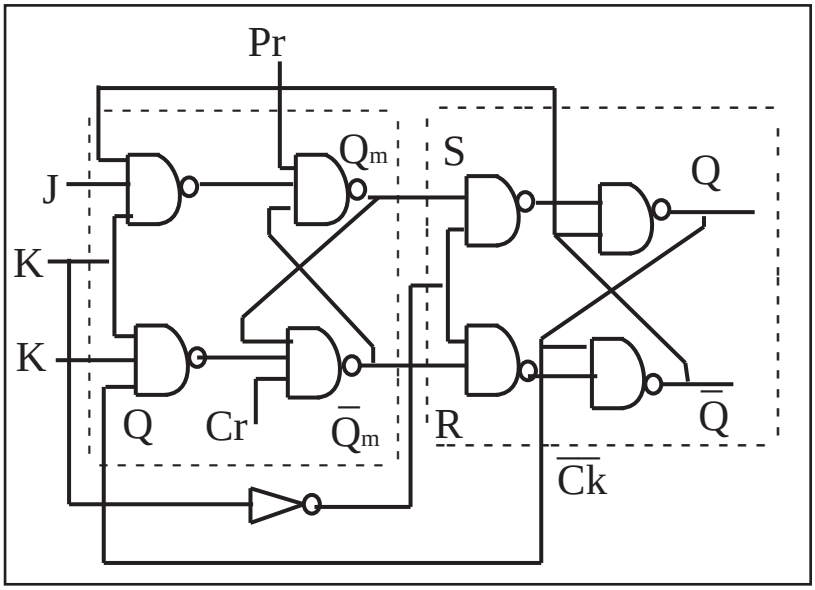
Excitation Table for JK

Q_n	Q_{n+1}	J_n	K_n
0	0	0	ϕ
0	1	1	ϕ
1	0	ϕ	1
1	1	ϕ	0

The Master Slave J-K Flip Flop

A master-slave J-K flip flop is a cascade of two S-R flip flops, with feedback from the output of the second to the inputs of the first.

Positive clock pulses are applied to the first flip-flop (master) and the clock pulses are inverted before these are applied to the second flip flop (slave), master is positive edge triggered and slave is negative edge triggered.

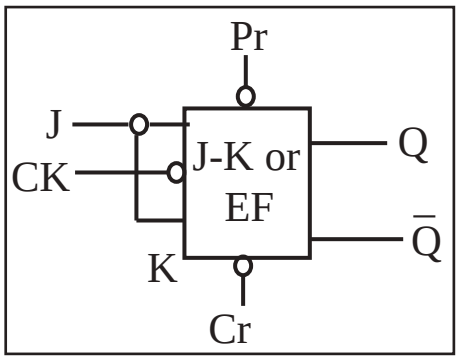


When CK = 1, the first flip flop is enabled and the output Q_m and $\bar{Q}_m$ respond to the input J and K according to the truth table of J-K. At this time, the second flip flop is inhibited because its clock is low($\overline{CK} = 0$), when CK goes low, the first flip flop is inhibited and the second flip flop is enabled. Therefore the output Q and $\bar{Q}$ follow the output Q_m and $\bar{Q}_m$. Since the second flip flop simply follows the first one, it is referred to as the slave and first one as the master. Hence this is referred to as Master-Slave (JK) flip flop.

T-FF

T-stand for Toggle

It is derived from J-K flip flop by joining J and K input.



Truth table

T_n	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

State Table

Q_n	T_n	Q_{n+1}
0	0	0
	1	1 ←
1	0	1 ←
	1	0

$Q_{n+1} = T_n \bar{Q}_n + \bar{T}_n Q_n = Q_n \oplus T_n$

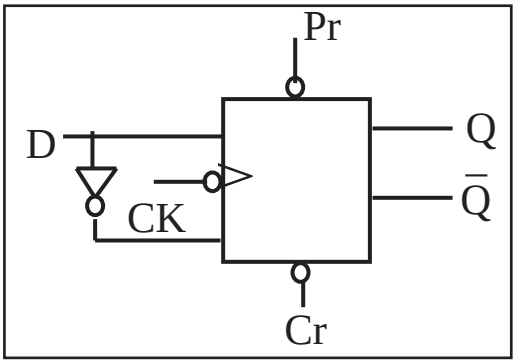
Excitation Table for T FF

Q_n	Q_{n+1}	T_n
0	0	0
0	1	1
1	0	1
1	1	0

D-FF

D stands for Delay

It is derived from JK flip flop by giving D to J and inverted input to K.



Truth Table for D- FF

D_n	Q_{n+1}
0	0
1	1

State Table

Q_n	D_n	Q_{n+1}
0	0	0
	1	1 ←
1	0	0
	1	1 ←

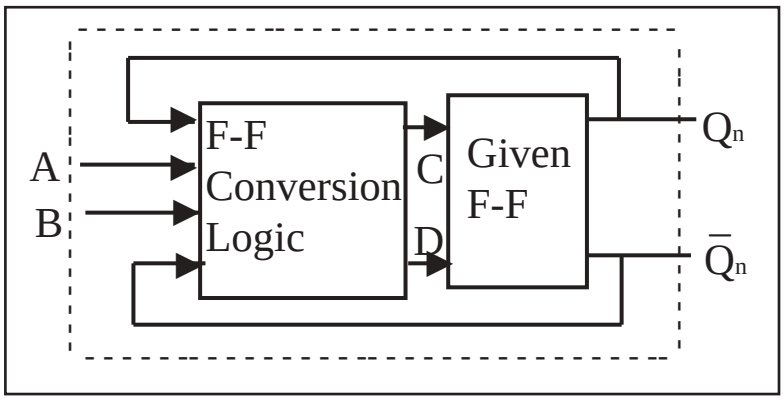
$Q_{n+1} = D_n$

Excitation Table for DFF

Q_n	Q_{n+1}	D_n
0	0	0
0	1	1
1	0	0
1	1	1

Conversion of FFS

Conversion of one FF to another is done by preceeding the given FF be a combinational logic circuit in following steps:



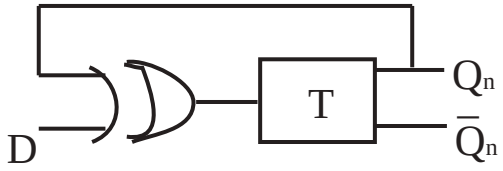
1. Write excitation table for available/given FF and FF to which it is to be converted.
2. Find expression for input C and D of FF in term of output Q_n and input of the target FF.
3. Draw the logic circuit based on expression.

Converting T to D flip flop

Q_n	Q_{n+1}	T_n	D_n
0	0	0	0
0	1	1 ←	1
1	0	1 ←	0
1	1	0	1

Expression for T in term of D and Q_n , we get

$T = \bar{Q}_n D + Q_n \bar{D} = D \oplus Q_n$

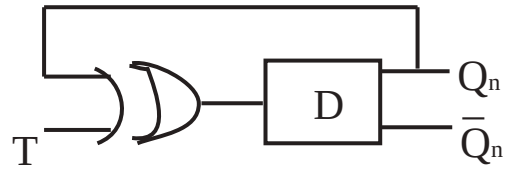


Converting D to T Flip Flop

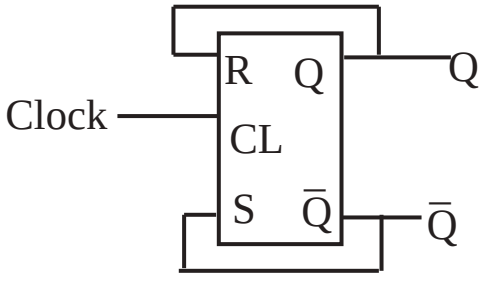
Q_n	Q_{n+1}	T_n	D_n
0	0	0	0
0	1	1	1 ←
1	0	1	0
1	1	0	1 ←

Expression for D in term of T and Q_n we get

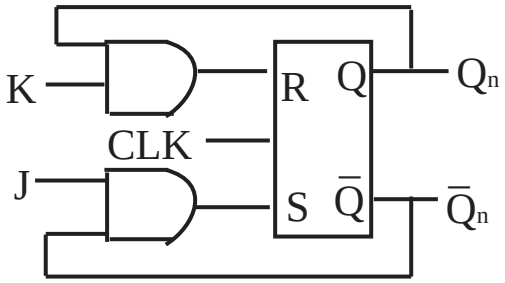
$D = \bar{Q}_n T + Q_n \bar{T} = T \oplus Q_n$



Converting R-S to T Flip Flop



RS to JK Flip Flop



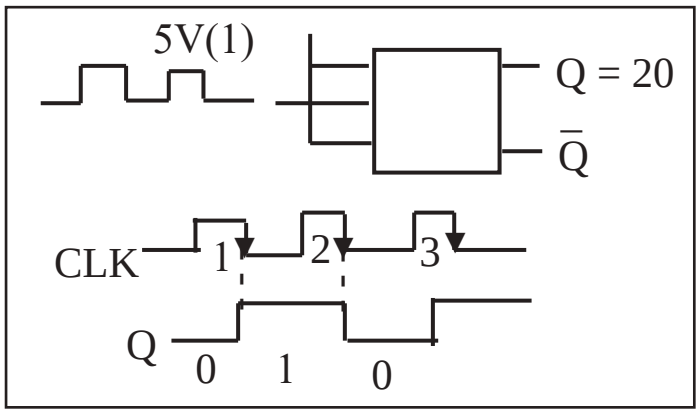
Uses of FFS

- Wide and extensive application in semi conductor memories counters, shift and storage registers.
- Used for binary addition, serial decoder, comparison and timing function.

Counters

Counters are used for measurement of frequency and its inverse, time period, sequencing of equipment operation, frequency division , and mathematical manipulation.

A clocked J-K flip-flop functions as a T-FF with both input J and K tied and kept HIGH(1) and when negative edge triggered toggles to the opposite state state $Q_{n+1} = \bar{Q}_n$



A single FF (J-K used as T) function as a divide by 2^N counter of N FF, it will be a divide by N, counter where N is a power of 2.

MOD of counter n = 2^N

N → No. of FFs

Hint : If there are 4 FFs, the modulus n = 16, this means a counter with 4 FFs can read a maximum decimal number that N FFs can read is $2^N - 1$.

Type Of Counters

1. Binary counter
2. Non-binary counter

If the maximum binary number is equal to 2^N, it is binary counter; otherwise it is a non-binary counter. MOD-16 is binary counter, whereas MOD 10 is not. Both Binary and non-binary counter are classified as synchronous and asynchronous counter.

Asynchronous

If the FFs are connected serially and the output of preceding FF clocks the succeeding FF, it is asynchronous counter as the change of states occurs one after the other. It also known as **ripple counter**.

In a **synchronous counter** all flip flop are clocked simultaneously with the clock input connected in parallel to the clock pulse.

In case of Asynchronous counter clock pulse period should be greater than Nt_{pd} . If in addition there is an interval T_s for **strobing**.

Clock period $T \geq N\ t_{pd} + T_S$

Maximum clock frequency is

$$f \leq \frac{1}{T} \leq \frac{1}{N\ t_{pd} + T_s}$$

where, N : no of flip flops

t_{pd} : Propagation delay of one FF.

t_s : Strobing interval

Design of ripple Counter, divide by N.

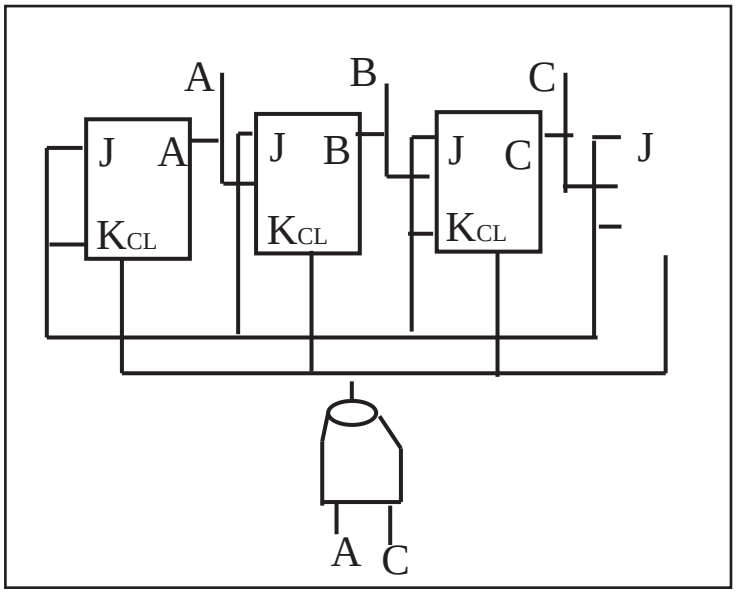
1. Decide the no. of FFs from the MOD number from the basic equation
   Modulus $n = 2^N$, N no. of FFs
2. Connect the FFs serially as a ripple counter.
3. Find the binary number N-1.
4. Connect all FF output that are 1 at N - 1 as inputs to a NAND gate.
5. Connect the NAND gate output to the the preset inputs of all the FFs which Q = 0 at the counter N - 1

   Steps 3 to 5 not required for required for pure Binary counter.

Example of MOD-10 Counter

Step 1 : Since MOD-10 is in between MOD-8 and MOD-16 counter so we need 4 FF.

Step 2 : MOD-10 counter will count 1001 (binary).



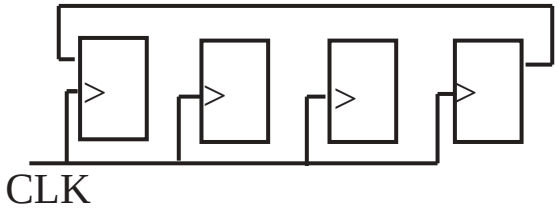
Step 3 : Whenever 1010 ($Q'_A\ Q_B\ Q'_C\ Q_D$) occurs, this should reset all flip flop output to 0000. So connect Q_A and Q_C to NAND gate input and give its output to clear input to all flip flop.

Glitch

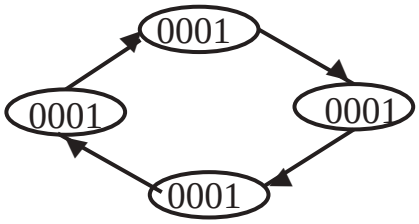
It is an unwanted spike. In the decade counter after decimal 9 or binary 1001 the counter does not recycle to 0000 immediately because of t_{pd} of NAND gate. It is unwanted spike for small duration known as Glitch.

Shift Register

Simplest of the shift register counters is a circulating shift register with output of last FF connected to input of 1st FF. It is also called aa RING COUNTER.



Suppose the initial state of the counter is $Q_3\ Q_2\ Q_1\ Q_0 = 1000$. The state diagram is shown below.



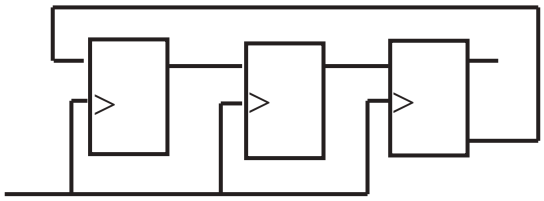
Flip Flops are connected so that information shifts from left to right and back around from Q_0 to Q_3

Q_3	Q_2	Q_1	Q_0	Clock
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3
1	0	0	0	4
0	1	0	0	5
.	.	.	.	.
.	.	.	.	.

This counter functions as a MOD-4 counter

Johnson Counter

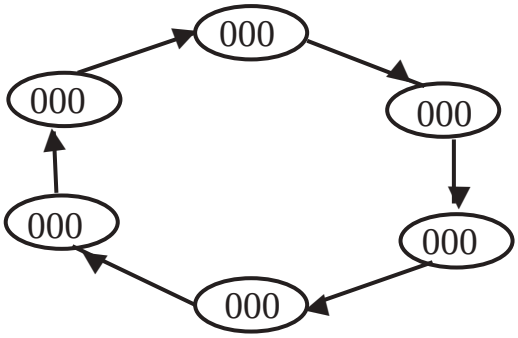
It is constructed like a normal ring counter except that the inverted output of the last FF is connected to D input of first FF. Three bit Johnson counter is shown.



The sequence table and state diagram for johnson counter are shown.

Q_2	Q_1	Q_0	Clock
0	0	0	0
1	0	0	1
1	1	0	2
1	1	1	3
0	1	1	4
0	0	1	5
0	0	0	6
.			
1	0	0	7
.	.	.	.
.	.	.	.

- This counter has six distinct state. Normally a n-state counter goes through 2n stages i.e MOD number = 2n.
- Waveform of each FF is square wave at 1/6th of the frequency of the clock.



Multiplexer

A multiplexer selects the one of N data input and feeds it into the single line. It is equivalent to single pole multi position switch. The selection of the input lines is controlled by a set of selection line. hence MUX is called the data selector.

Parts of MUX

(a) data or input line
(b) Selection or control line
(c) Output line

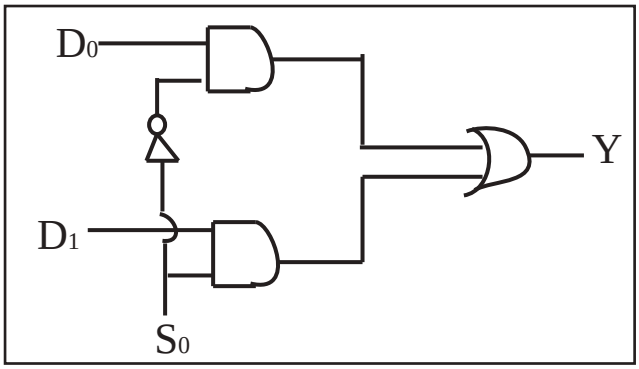
Uses of MUX

1. Data selection
2. Time divison multiplexing (TDM)
3. Function generation
4. Universal logic circuit- SOP

Input MUX

Basically a MUX consist of an AND and OR gate circuit with an inverter in the select line. There is one AND gate for each input.

D_0, D_1,D_2 => refer to input data
S_0, S_1, S_2 => refer to Control data
Y_0,Y_1,T_2 => refer to output data



The Boolean functions is $Y = D_0 \overline{S}_0 + D_1 S_0$

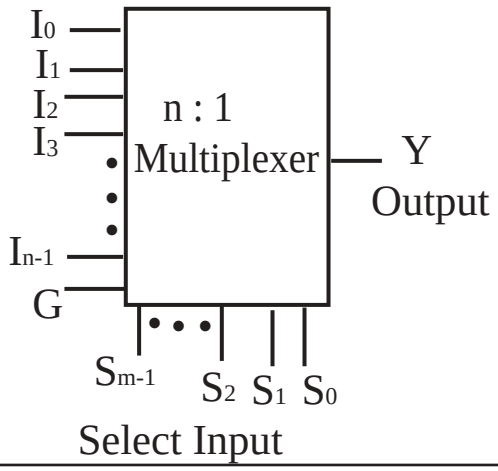
Truth Table

S_0	Y
0	D_0
1	D_1

We see from the truth table that so controls or selects the output y.
If $S_0 = 0$, $Y = D_0$
If $S_0 = 1$, $Y = D_1$
An AND-OR gate is equivalent to NAND-NAND gate and hence we can drive any logic function.
Number of select line $\log_2 n$
where n = number of input/output for MUX/DEMUX.

Design of Multiplexers

The multiplexer is a special combinational circuit that is used most widely. It is a logic circuit that gates one out of several inputs to a single output. The input selected is controlled by a set of select inputs.



Truth table of a 4 : 1 multiplexer

Select S_1	Input S_2	Output (Y)
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$y = \overline{S}_1 \overline{S}_0 I_0 + \overline{S}_1 S_0 I_1 + \overline{S}_1 \overline{S}_0 I_2 + S_1 S_0 I_3$

Combinational Logic Design Using Multiplexers

In this method, one of the variable called the residue is applied to the data input.

Example : f (A, B, C, D) = Σ(0, 1, 5, 7, 10, 14, 15)

Solution : This is a variable function.

Number of selection line = 4 - 1 = 3

and input $(2)^3 = 8$ line

Step 1 : The input to the multiplexer are listed I_0 , I_1, I_2, I_3, . . . I_7

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{D}$	0	1	2	3	4	5	6	7
D	8	9	10	11	12	13	14	15

where, D(MSB) and A(LSB). 0 to 15 assigned to D' to D such that corresponding to number from 0 to 15, either D = 1 or D = 0. If D = 1 then again put it to 2nd row from 8 to 15 otherwise from 0 to 7.

Now (ii) circle the representation of function in the above table.

Now, if two column are not circle, apply '0' to the corresponding MUX input.

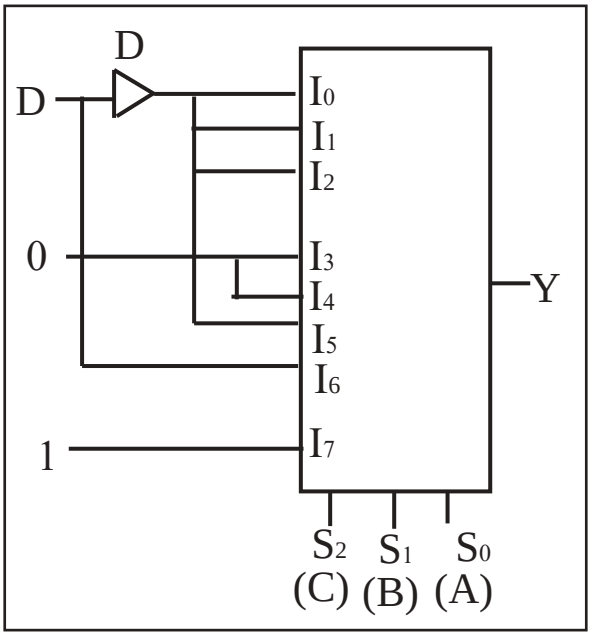
- If two columns are circle, apply '1' to the MUX input.
- If the top row of column is circled, apply D' to the corresponding MUX input.
- If the bottom row of column only is circled, apply 'D' to the corresponding MUX input.

From above we can find that

$I_0 = \bar{D}$, $I_2 = D$, $I_4 = 0$, $I_6 = D$

$I_0 = \bar{D}$, $I_3 = 0$, $I_5 = D$, $I_7 = 1$

So final realization with MUX

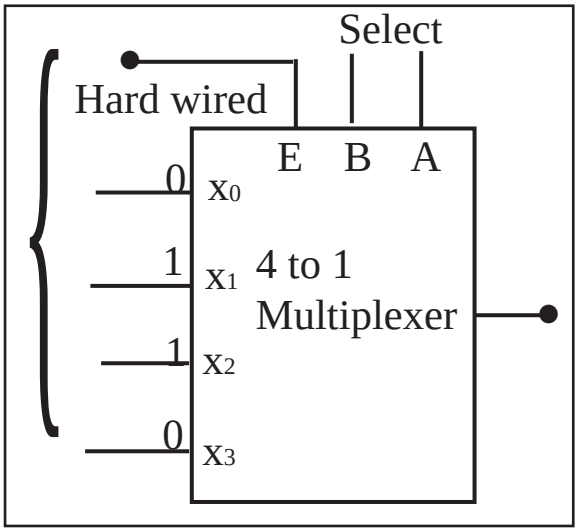


XOR Function Realization using (4 × 1) MUX

$Y = A\bar{B} + \bar{A}B$

We have to use A, B for selection line. Whenever AB' = 1; or A'B = 1, output

is high, otherwise output is zero.



Demultiplexers (Date Distributors)

Demultiplexer functions opposite to that of MUX. It receives information on a single line and distributes it to possible 2n lines where n is the number of selection lines.

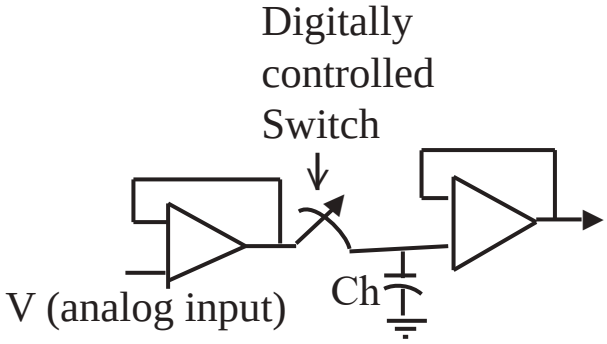
Decoders

A binary word length of n bits can contain upto 2^n distinct elements of coded information of n-lines and feeds them to 2^n unique output lines after conversion.

Comparison of Multiplexer and Decoder

- Only one decoder is necessary to generate all min terms. However, the number of OR gates required is equal to the number of outputs.
- One multiplexer is required for each output function.
- So if the outputs are small in number, multipliers are used. Decoder 1C's are used for large output function.

S/H Circuit



In practice, the sampling of an analog signal is performed by a simple and hold circuit. The sampled signal is then quantized and converted to digital form. Usually, the S/H is integrated into the A/D converter.

The S/H is a digitally controlled analog circuit that tracks the analog input signal during the sample node, and then holds it fixed during the hold mode to the instataneous values of the signal the time the syatem is switched from the instantaneous value of the signal at the time the system is switched from the sample mode to the hold mode. Figure (b) shows the time-domain response of an ideal S/H circuit.

The goal of the S/H is to continuously sample the input signal and then to hold that value constant as long as it takes for the A/D converter to obtain its digital representation. The use of an S/H allows the A/D converter to operate more s;\lowly compared to the time actually used to acquire the sample. In the absence of a S/H, the input signals must not change by more than one-half of the quantization step during the conversion, which may be an impractical constricting consequently, the S/H is crucial in high resolution digital conversion of signals that have large bandwidths.

An ideal S/H introduces no distortion the conversion process and is accurately modeled as an ideal sampler. However, time-related degradations such as errors in the periodicity of the sampling process nonlinear variations in the duration of the sampling aperture, and changes in the collage held during conversion do occur in practical devices.

The A/D converter begins the conversion after it receives a convert command. The time required to complete the conversion should be less than the duration of the hold mode of the S/H. Furthermore, the sampling period T should be larger than the duration of the sample mode and hold mode.

In the following sections we assume that the S/H introduces neglible errors and we focus on the digital conversion of the analog samples.

Analog to Digital and Digital to Analog Converters

Digital to Analog Converters

The input to a D/A converter is an N-bit binary signal. The analog output voltage V_0 of an N-bit straight binary D/A converter is related to the digital input by the equation.

$$V_0 = K(2^{N-1} . b_{n-1} + 2^{N-2} . b^{n-2} + ...)$$

where, K = Proportionality factor

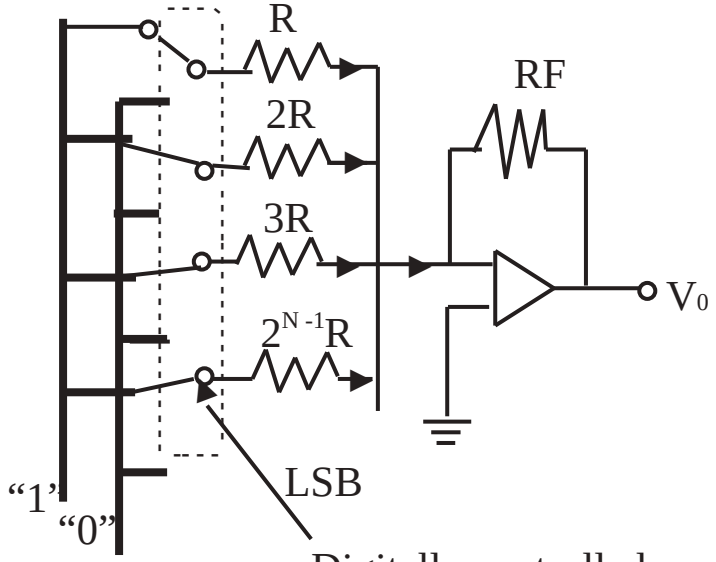
b_n = 1 if the nth bit of the digital input is 1

= 0 if the nth of the digital input is 0

Types of D/A Converters

1. Weighted-resistor D/A converter and
2. R-2R ladder D/A converter

Weight-Resister D/A converter



Resister for MSB = R

Resister for LSB = 2^{N-1}. R

$$V_0 = -V_R \left(\frac{R_F}{R} b_N + \frac{R_F}{2R} b_{N-1} + \ldots . R_F \frac{b_{N-N}}{2^{N-1} R} \right)$$

Example : 4 bit D/A, V(1) = 1V, R_F = 8R. Obtain analog output voltage for 0101?

$$V_0 = -1 \left(\frac{8R}{R} \times 0 + \frac{8R}{2R} \times 1 + \frac{8R}{4R} \times 0 + \frac{8R}{8R} \times 1 \right)$$

$$= -[4 + 1] = -5$$

D/A Performance Characteristics

1. FSV (Full Scale Voltage) : It represents maximum output voltage for the DA converter and is obtained when all bits of digital input are 1.

The output for any bit is $e_0 = V_R / 2^n$

Where n = no. of bits.

$FSV = V_R [1 - (1/2^n)]$

2. Resolution

$$\% \text{ Resolution} = \frac{\text{Step size}}{FSV} \times 100 = \frac{1}{2^{n-1}} \times 100$$

3. Accuracy : It is the error between the actual output of DA converter to the expected or theoretical output and expressed as percentage of FSV.

If the converter has an accuracy of ± 0.1% for FSV of 10V, the minimum error for any output voltage is [(10/100) × 0.1] = 10 mV. Ideally the accuracy should be = ± [1/2] LSB

4. Monotonicity : It means that the output increase for an increase of input or decrease for decrease of input. The output should not decrease for increase of input.

5. Settling Time : It is the time taken by DA converter to settle within ±[1/2] LSB of its final value.

Major Component of the Binary Weighted Resistance DAC :

(a) A weighted resistor networ, R to 2^{n-1} R

(b) n switches, one for each bit applied bit input.

(c) A reference voltage V_{ref}

(d) A summing element.

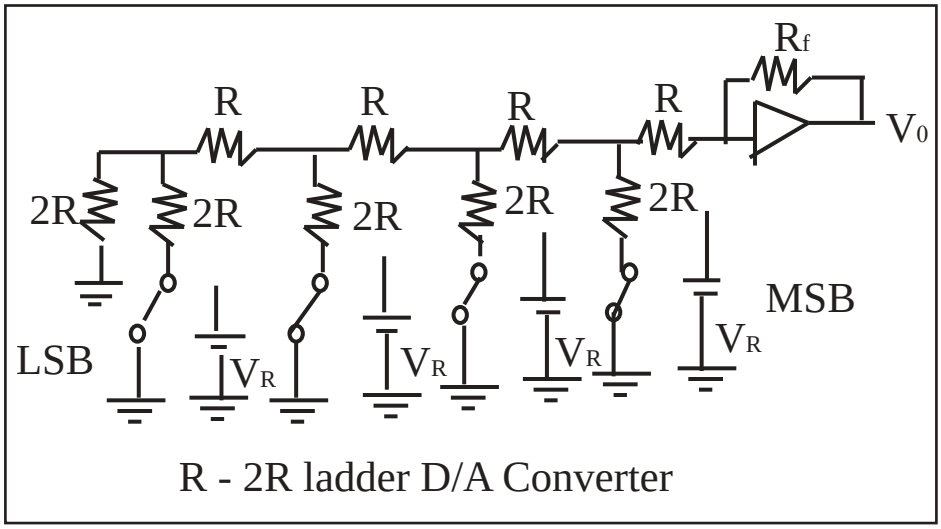
Defects : The chief detect of weighted binary DAC is that the resistor values increase in multiples of 2.

If the value of MSB is 2 KΩ. Then for a 10 bit, the value for LSB is 2^9. 2K = 1.024 MΩ

It is difficult to obtain high precision at very high values. It is also difficult to fabricate high value resistance by integrated circuit methods. This is overcome by the ladder type DA converter.

R-2R Ladder Network

In this, only two values of resistors are used.



R - 2R ladder D/A Converter

$V_n = V_R (2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + ... b_0) / 2^N$

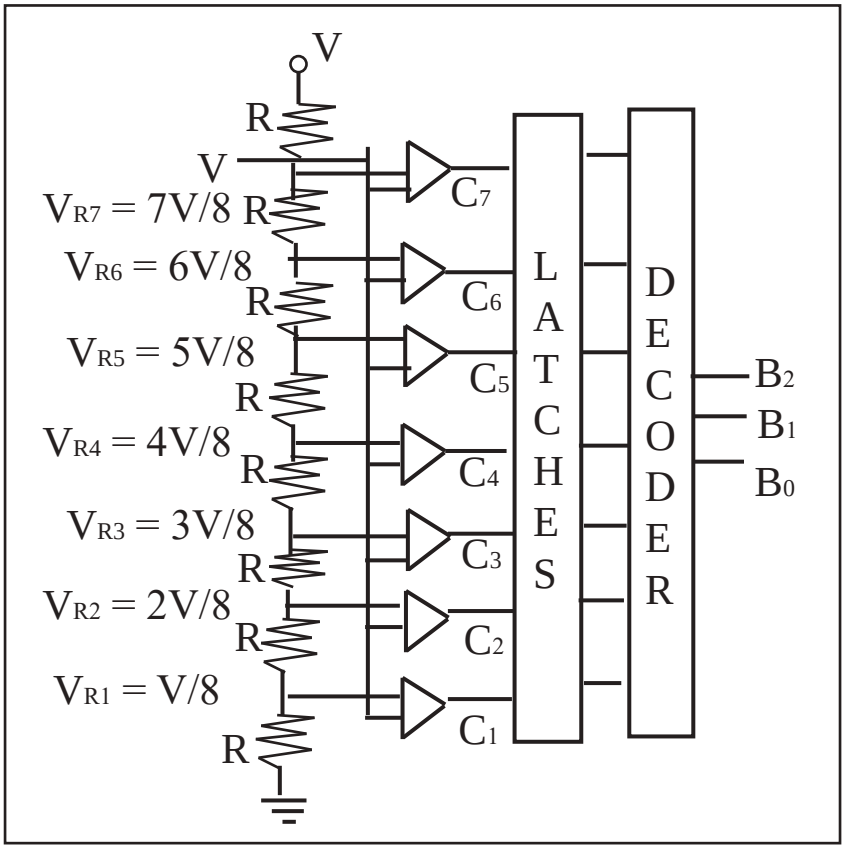
The number of resistor required for an N-bit ladder D/A converter is 2N in the case of R-2R ladder D/A converter whereas it is only N in the case of weighted-resister D/A converter.

Analog-To-Digital Converters : Types of ADC

1. Parallel-comparator/flash/simultaneous A/D

• Simplest in concept and fastest conversion time.

• Disadvantages are rapid increase in the number of comparators with the number of bits, $(2^N - 1)$ comparators are required for an N-bit converter.

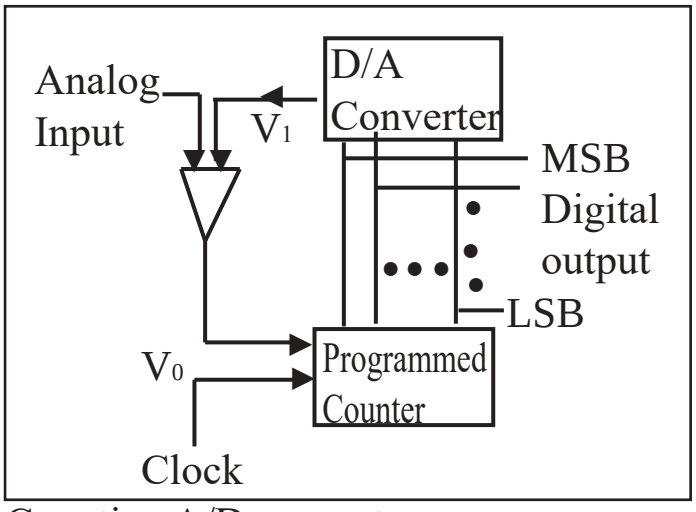


2. Successive Approximation A/D converter

• For N-bit converter the number of clock pulses required would be N.

• Slow than the parallel comparator A/D

Offset voltage = 1/2 LSB - 0.5



3. Counting A/D converter

the maximum number of clock pulse required conversion is 2^N for an N-bit A/D converter. This converter is slower than the other two converters discussed earlier

4. Dual-slope A/D converters

Major component of a dual-slope A/D converter

1. An integrator 2. A comparator
3. A binary counter 4. A switch driver

Conversion time of ADC

1. Counter of Ramp type ADC

$$t_c = \frac{2^n - 1}{f} = (2^n - 1)\,\tau$$

2. Successive approximation ADC

$$t_c = \frac{[n]}{.f} = n\tau$$

3. Dual slope ADC

Slowest conversion time

4. Flash ADC

Fastest converting time $t_c = (1/f)$

- Conversion time independent from no. of bit.
- The number of Comparator = $2^n - 1$

where f = clock frequency

Aperture Time

Aperture time is called the Maximum allowable conversion time t_c .

$$t_a = \frac{1}{\omega(2^n - 1)}$$

where, ω = angular frequency of signal applied
n = number of bit for ADC
t_a = aperature time.

Basics of Number System

Number Systems and Codes

A number system is language system consisting of an ordered set of symbols called digits with rules defined for addition, multiplication, and other mathematical operation. The radix or base of a number system specifies the actual number of digits included in its ordered set. Further, a number system allow for number (collection digits) to have an integer and a fractional part set apart by a radix point.

There are various number system based on radix which are required for various purposes:

1. Decimal number system (i.e) with 0, 1, 2 , . . . 9), base-10

2. Binary number system (i.e with 0,1), base-2
3. Trinary number system (i.e with 0, 1, 2), base-3
4. Quinary number system (i.e with 0, 1, 2, . . ., 4), base-5
5. Octal number system (i.e with 0, 1, 2, . . . 7) base-8
6. Hexadecimal number system (i.e with 0, 1, 2,..., 9, A, B, ... F(15), base-16 (H)

Binary Number System

Almost all digital computers and systems are based on binary (two state) operation e.g a switch, magnetic core tape, punched card, tape recorder, transistor action cutoff or saturation.

- The number system with base (or radix) two is known as the binary number system.
- Two symbols are used to represent numbers in this system and there are 0 to 1, known as bits.
- It is potential system, that is every position is assigned a specific weight.
- A group of four bits is known as **nibble**, and a group of eight bit is known as **byte.**

Binary - To - Decimal Conversion

Any binary number can be converted in to its equivalent decimal number using the weights assigned to each bit position.

Example :

$(11101)_2 = 1(2)^0 + 0.(2)^1 + 1.(2)^2 + 1.(2)^3 + 1.(2)^4$

$= 1 + 0 + 4 + 8 + 16 = 29$ (decimal)

So, $(11101)_2 = (29)_{10}$

In case we have from like $(111.01)_2$ then we have to manipulate like this

$(111.01)_2 = 1.(2)^0 + 1.(2)^1 + 1.(2)^2 + 0.(2)^{-1} + 1.(2)^{-2}$

$= 1 + 2 + 4 + 0 + (1/4) = (7.25)_{10}$

Decimal to binary conversion

Any decimal number can be converted into its equivalent binary number. The conversion is obtaning by continuous division by 2 and keeping track of the conversion is affected by continuous multiplication by 2 and keeping track of the integers generated for.

Example : For this $(13)_{10}$

Carry			
2	13		
2	6	1	LSB
2	3	0	
2	1	1	
	0	1	MSB

So we have $(13)_{10} = (1101)$
For converting $(0.65625)_{10}$ into binary
$0.65625 \times 2 = 1.131250$ (keep integer part, i.e. 1) MSB
$0.3125 \times 2 = 0.625$ (keep integer part, i.e 0)
$0.625 \times 2 = 1.25$ (keep integer part, i.e 1)
$0.25 \times 2 = 0.5$ (keep integer part, i.e 0)
$0.5 \times 2 = 1.0$ (keep integer part, i.e 1) LSB
so $(0.65625)_{10} = (0.10101)_2$

Sign-Magnitude representation

- Plus (+) sign is used to denote a positive number and minus (-) sign for denoting a negative number in decimal numbers.
- In digital world, to represent sign we represent the same in term of Bit (0 or 1). An additional bit is used as sign bit, and it is laced as the most significant bit.

  0 = is used to represent a positive number
  1 = is used to represent a negative number
  Example : 8 bit signed number 01000100 give positive number of value $(1000100)_2 = (68)_{10}$. the left most 0 (MSB) indicate that the number is positive.
  On the other hand (11000001) represent negative number of value (-65)

One's Complement Representation

In a binary number, if each 1 is replaced by 0 and each 0 by 1, the resulting number is known as one's complement of the first number.

Both the number are complement of each other.

If one of these number 1's positive, then the other number will be negative with the same magnitude and vice versa

(0101) → (+5) whereas
(1101) (-5)

Two's complement representation

If 1 is added to 1's complement of binary number the resulting number is known as the two's complement of the binary number.

Example : Find 2's complement of (0101)

$0101 \xrightarrow{\text{1's complement}} 1010$

$1010 \xrightarrow{\text{add 1}} 1011$ (2's complement)

$0101 \rightarrow (+5)_{10}$

therefore (1011) represent $(-5)_{10}$

2's representation

If the LSB of a number is 1, its 2's complement is obtained by changing each 0 to 1 and 1 to 0 except the LSB.

If the LSB of a number is 0, its 2's complement is obtained by scanning the number from LSB to MSB bit by bit as they are up to and including the occurrence of the first 1, and complement all other bits.

Binary Arithmetic

Binary Addition

A	B	S(sum)	C(carry)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

$S = A\overline{B} + \overline{A}B$

Where, S → Sum of bit A and B

C → Carry generated after addition of A and B

Figure of Merit

The figure of merit of a digital IC is defined as the product of speed and power. A low value of speed power product is desirable.

Fan Out

This is the number of similar gates which can be driven by gate. High fan out is advantage because it reduces the need for addition drivers to drive more gates.

Current and Voltage, Parameters

Current parameters are I_{OH}, I_{OL}, I_{IH}, I_{IL} and voltage parameters are V_{OH}, V_{OL}, V_{IH}, V_{IL}.

Noise Immunity

As discussed earlier i.e. NM_H and NM_L, noise may cause the voltage at the input to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation. The circuit ability to tolerate noise signal is referred to as the noise immunity.

Operating Temperature

The temperature range in which an IC functions properly must be known. The accepted temperatures are 0 to 70ºC for consumer and industrial applications and -55ºC and 25ºC for military purpose.

Power Supply Requirements

The supply voltage(s) and by an IC are important characteristics required to choose the proper power supply.

Flexibility Available

Various flexibilities are available in different IC logic families and these must be considered.

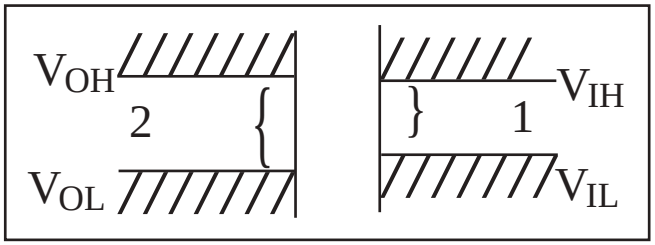
* *Wire logic capability:* the output can be connected together to perform additional logic without any extra hardware.
* *Availability of complement output:* This eliminates the need for additional inverters.

Digital Signals Voltage Levels

where,

V_{OH} = Output voltage at high signal

V_{OL} = Output voltage at low signal



V_{IH} = Input voltage at high signal; V_{IL} = Input voltage at low signal

(1) and (2) forbidden region.

* If Input voltage to any logic gate is less then V_{IH}, then input may be considered as low (i.e. = 0).
* If input voltage to any logic gate is greater then V_{IH}, then in out may be considered as high (i.e. = 1).
* If output voltage of any logic gate is greater then V_{OH}, then output may be considered as high (i.e. = 1).
* If input to any logic gate lies in region (1) then input level is considered as forbidden similarly if outpuit signal of any logic gate lies in region (2) then output is in forbidden region, so we cannot say whether output is high or low.

  $NM_L = V_{IL} - V_{OL}$ $\qquad$ $NM_H = V_{OH} - V_{IH}$

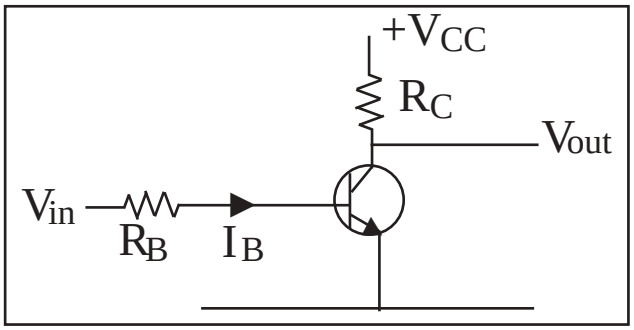
  where, NM_H = Noise margin in high state.

  NM_L = Noise margin in low state.
* Large noise margin better logic gate i.e. less effect of noise.
* FOM = Figure of Merit $\qquad$ P_{DP} = Power dissipation

  T_D = delay $\qquad$ $FOM = T_D \times P_{DP}$

RESISTORS-TRANSISTOR LOGIC (RTL)

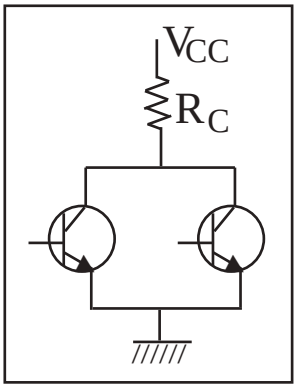
* RTL logic was the most popular form of logic in common use before the development of IC's.
* RTL circuit consists of resistors and transistors.
* The basic RTL based NOR gate



Logic Operation

Input representing the logic levels are voltage corresponding to low level should be low enough to drive the corresponding transistor to cut-off. Similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturated.

DIRECT-COUPLED TRANSISTOR LOGIC (DCTL)



In the RTL, if the base resistors R_B are omitted we obtain, DCTL, in which input is directly coupled to Bases.

Disadvantage

Voltage corresponding to 1 → 0.8v

Voltage corresponding to 0 → 0.2v

Then logic Swing ; 0.8-0.2 = 0.6v

This gives very low noise margin.

Also, it is having problem of current hogging this problem may not occur if all transistors have same input characteristic but, unfortunately, the input characteristics differ due to the manufacturing tolerance of different IC. Owing to this difference, the saturation voltages of the load transistors may be different.

Let V_{BE} voltages of the transistors corresponding to saturation be 0.78, 0.79, 0.80 V. The first transistor when it enters saturation, will not allow other transistor to enter saturation and will take whole of the current supplies from the driver gate. This is known as current hogging.

INTEGRATED INJECTION LOGIC (I^2L)

* It is simple and uses very small silicon area, consumes very little power.
* Easier and cheaper to fabricate, so suitable for MSI and LSI.
* It uses the concept of merging the components i.e. one semi conductor region is part of two or more device, so also called as (MTL) merged transistor logic.

DIODE-TRANSISTOR LOGIC (DTL)

* DTL make use of diode AND or OR gate and transistor invertor in series for making it to be used as NAND and NOR operation.

* DTL is some what more complex than RTL, but due to high fan out and improved noise margin, it has replaced RTL.
  It is slower speed, poor noise margin.

Propagation Delays

Delays are associated with the turning-on and the turning-off of the output transistor. While turning on, any capacitance shunting the output of the gate discharges rapidly through the low impedance of the output transistor in saturation. On the other hand, at turn-off, the shunt capacitor must charge through the pull-up resistor R_e in addition to the storage time delay. The turn off delay is larger than the turn-on delay.
The propagation delay time of commercially available DTL gates are of the order of 30 to 80 n sec.

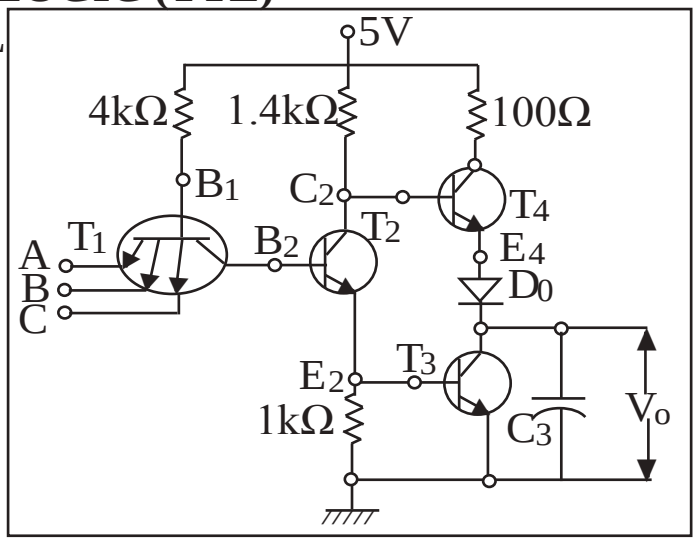
HIGH-THRESHOLD LOGIC (HTL)

Due to the presence of Electric motors, on-off control circuit, high voltage switching the noise level is quite high and the logic family discussed so far, don't perform the intended function.
For this purpose, DTL gates has been redesigned with a higher supply voltage (15 V).
Diode have been replaced by a zener diode with V_z = 6.9 V and resistances have been increased so that Approximately the same current are obtained as in DTL.

* The propagation delay time is adversely affected due to large resistance value.
* The noise margin obtained with this circuit is typically 7 V.

TRANSISTOR TRANSISTOR LOGIC (TTL)

Difference between TTL and DTL
The input diode in DTL are replaced by emitter-base junctions of multiple-emitter transistor, which is easily and economically fabricated IC.



Totem-Pole Transistor

Q_4 is used because they produce low output impedance which act as power driver or power buffer.

TTL Based NAND Gate and its Operation

Diagram of a TTL NAND gate with totem-pole output. Active pull up is provided by T_4, D_0 and 100 ohm resistor.

Condition

At least one input is LOW. The emitter-Base junction of T_1 corresponding to the input in the low state is forward biased making voltage of (B_1). $V_m = 0.2 + 0.7 = 0.9$ V

This value of V_m causing T_2 and T_3 to turn off and hence V_{out} charged to V_{cc} so $V_{out} = V_{cc}$.

High Power and Low Power TTL

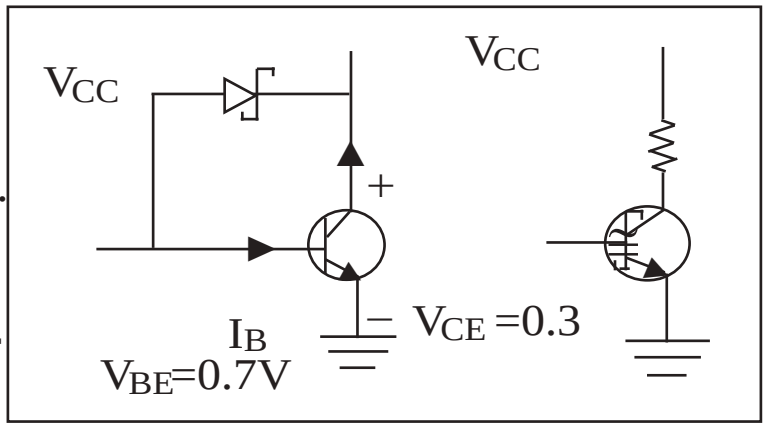
If we reduce the values of the resistance used it will result in more flow of current and the switching speed of the circuit is increased by factor of 2.

By increasing resistance of the circuit the power dissipation is decreased by factor of 10 and speed by factor of 3 as compared to that of a standard TTL.

SCHOTTKY TTL

Speed limitation of TTL is mainly due to the turn-off time delay involved in transistor while making transition from saturation to cut-off (storage time delay). This can be eliminated by replacing the transistors of TTL gate by schottky transistor.

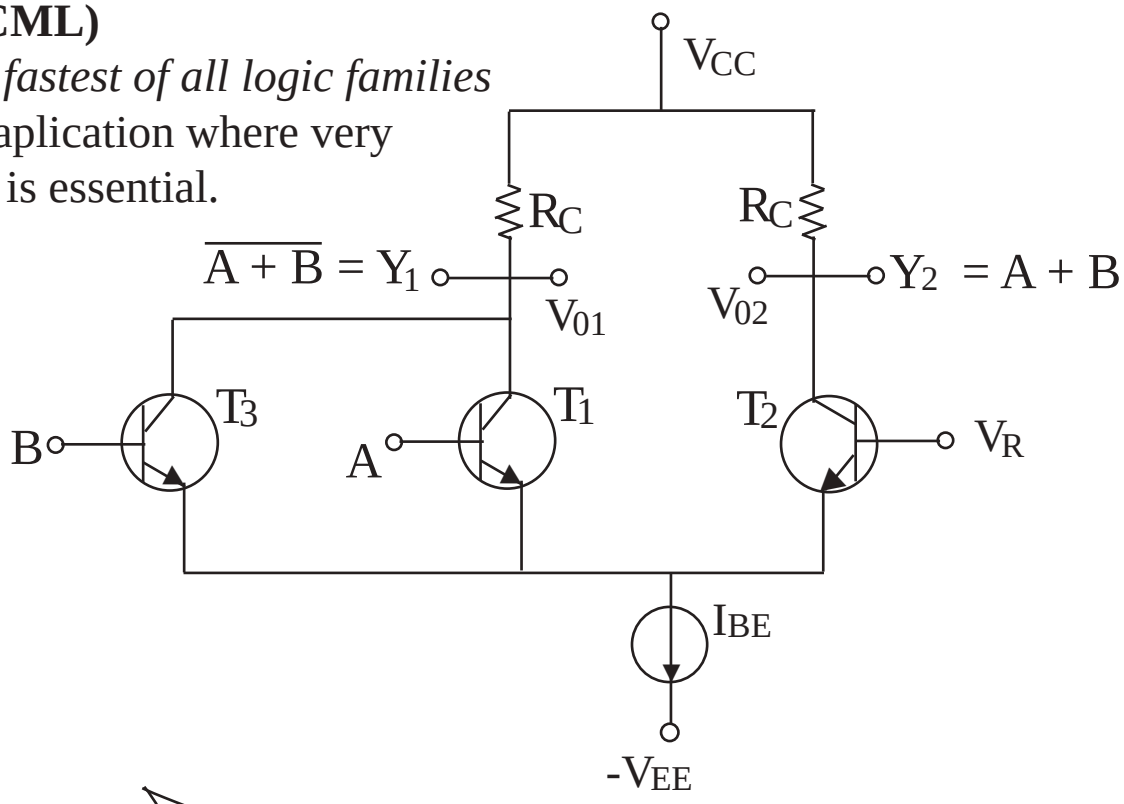
This schottky transistor prevent transistor from entering saturation and hence, there is saving in turnoff time. (Schottky diode is clamped between base and collector). A schottky diode works faster as compare with commercial

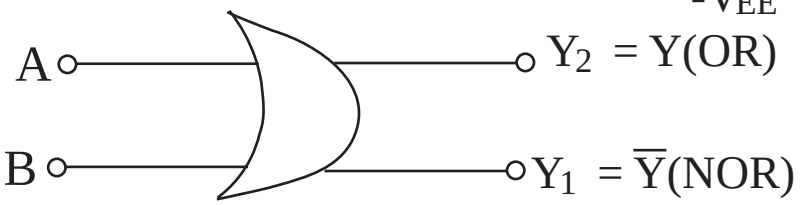


diode because of fact the electron which have crossed the junction and entered the metal, when the current is flowing are similar to the cond-ction electrons of the metal.
Reverse recovery time for schottky diode is few p sec rang.

EMITTER-COUPLE LOGIC (ECL) OR CURRENT MODE LOGIC (CML)

ECL is *the fastest of all logic families* so used in aplication where very high speed is essential.





(b)

* High speed is possible in ECL because the transistors are used in difference amplifier either in active or cut-off region and thereby the storage time is eliminated.
* ECL is realized using difference amplifer in which the emitter of the two transistors are connected so called emitter-coupled logic.
* Most of the super fast computer and high speed special purpose computer used these ECL logic families.
* Emitter follower are used for d.c. level shifting of the output. So, that V(0) and V(1) are same for the input and the output.

* Two output Y_1 and Y_2 are available in this circuit. Which are complementary. Y_1 correspondent to NOR logic and Y_2 to OR logic.
* In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply.
* Fan out is large-why.
* If all the input are low, the input transistors are cut-off. Therefore, the input resistance is very high. On the other hand, if an input if HIGH, the input resistance is that of emitter followers which is also high. So, input impedance is always high.
* The output resistance is either that of an emitter followers or the forward resistance of a diode, which is always low, because of low output impedance and high input impedance, *the fan out is large.*
* The output of two or more ECL gates can be connected to obtain additional logic without using additional hardware.

Unconnected Input

If any input of an ECL gate is left unconnected the corresponding E-B junction of the input transistor will not be conducting, so can be treated as logical 0.

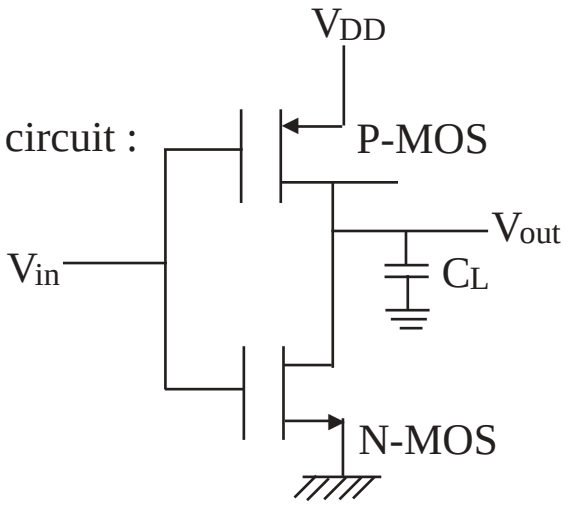
MOS-LOGIC

* High density of fabrication and low power dissipation.
* MOS devices used in logic circuits, are only p or n-channel.
* CMOS lowest power dissipation.

CMOS Based Inverter

This is basic building Block for CMOS circuit :

Circuit diagram :



Operation

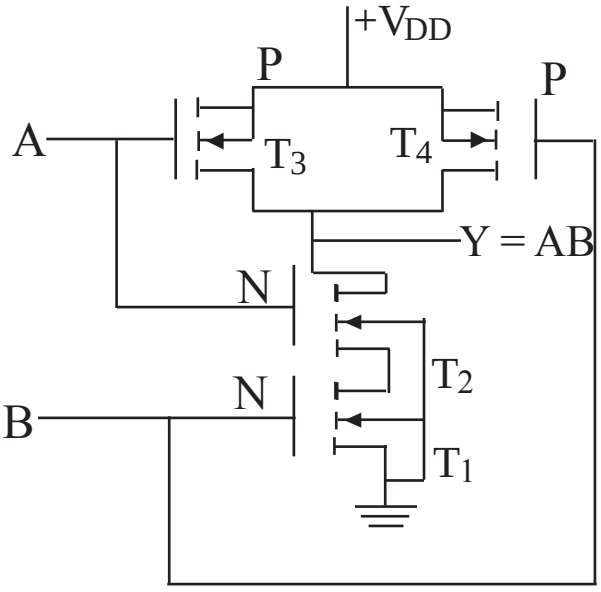
When $V_{in} > (V_{th})$ (V_{thn}) → threshold voltage for NMOS)
NMOS turned ON and V_{out} is '0' as Capacitor discharged to ground.

When V_{in} low which cause PMOS to turn ON and NMOS is turn off, the Capacitor starts charging by supply voltage V_{DD}.

So, $V_{in}(1) \rightarrow V_{out}(0)$ $V_{in}(0) \rightarrow V_{out}(1)$

* No static power dissipation as at a time only one of the MOS, either PMOS or NMOS is turn ON so there is no direct path from V_{DD} to ground, so static power consumption is zero (ideally).
* During transition from zero to one (for input signal), there will be voltage level at which Both NMOS and PMOS turned ON, giving direct path from supply to ground so there is power dissipation. This power loss is termed as *Dynamic Power dissipation.*
* *Dynamic Power dissipation* is given by $P_d = (1/2) C_L V_{DD}^2 f$
  where, P_d = Dynamic power Dissipation
  V_{DD} = Supply voltage
  f = Switching frequency C_L = Load Capacitor
* Strongly depends on Supply voltage, so to reduce power dissipation reduce supply voltage, but to that limit so that noise can't effect circuit operation.
* Reduce load capacitance.
* Reduce the frequency of operation but this will reduce frequency at which we want to operate my circuit.

CMOS-NAND GATE



A 2-input CMOS NAND gate

Operation

When Both Signal (A and B) are high, Both NMOS turned ON and output goes to zero. For rest of combination at least one of the NMOS is OFF and at least one PMOS is ON which cause V_{out} to go high.

Realization of Any Boolean Function in CMOS

Realization of Boolean Function in CMOS needs following steps.

Complement the function to be realized.

If product term is there, then use two NMOS in series and if add term is there then use to NMOS in parallel.

If NMOS is found then what is series in NMOS, just put them in parallel using PMOS. And what is parallel in NMOS just put them in series using PMOS.

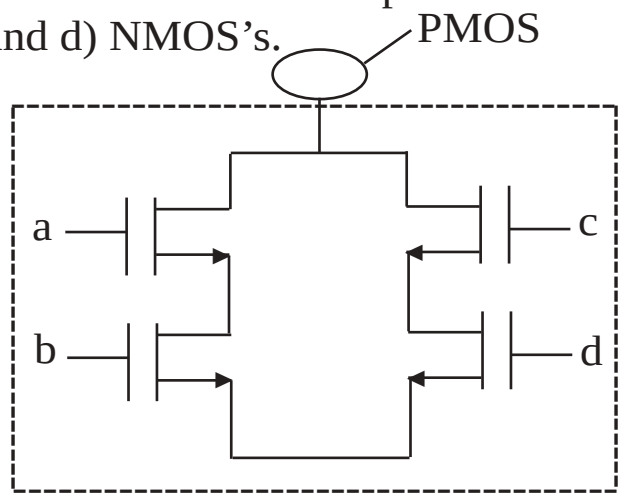
Example : $f = \overline{ab + cd}$

Step 1 : Find complement of this function. $\overline{f} = abcd$

Step 2 : There is two term (ab) and (cd) which is product term, it is realized by series NMOS separately.
Then for OR ing ab and cd used two NMOS combination in parallel.

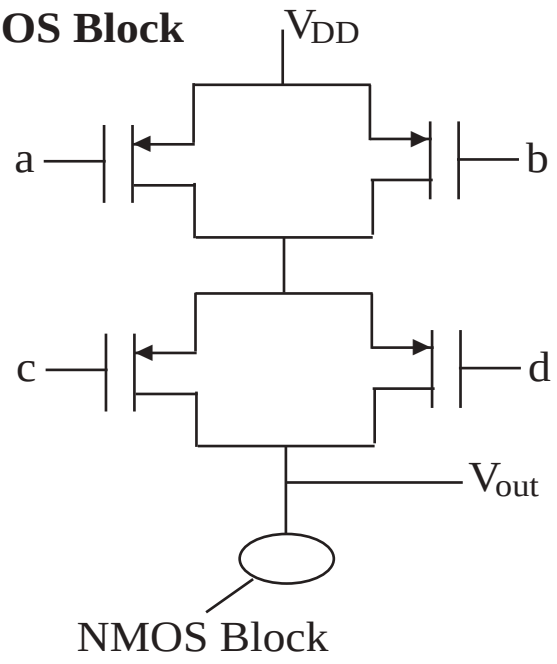
Step 3 : To find PMOS Block, just to do manipulation. Whatever there is in NMOS. For example (a and b) NMOS are in series put them in parallel (in PMOS). Similar for (c and d) NMOS's.

After this since (a and b) and (c and d) are parallel in NMOS, then put them in series for (PMOS) version.



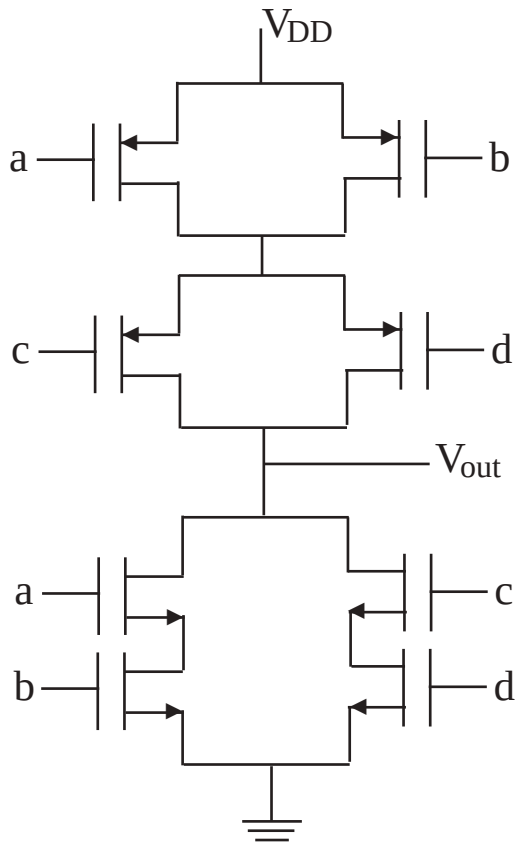
NMOS Block

PMOS Block



NMOS Block

Full Schematic

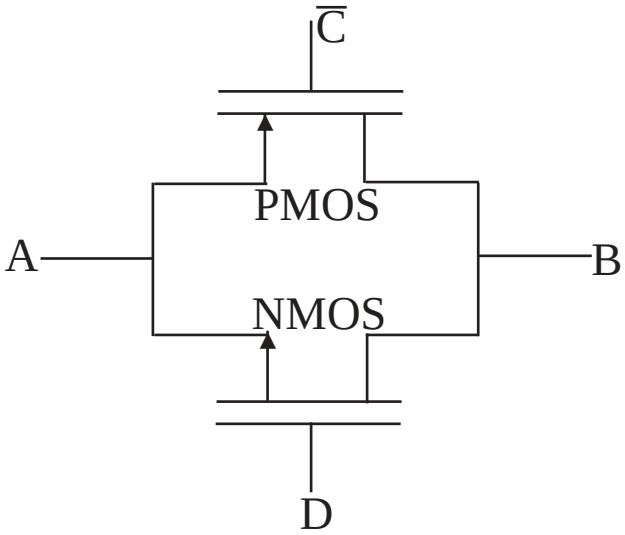


WIRED LOGIC

The output impedance of a CMOS gate is 1 k and connecting gates directly in parallel would draw large current (mA). A special circuitry is devised to achieve wired-OR connection. This is known as **transmission gate.** Wired logic must not be used for CMOS logic circuit.

CMOS Transmission Gate :

Circuit Diagram



* Controlled by gate voltage C and C'. When C = 1 and C' = 0 assume A = V(1), then T_1 is OFF and T_2 conducts in the ohmic region. So T_2 behaves as a small resistance connecting the output to the input and B = A = V(1). If A = (0), T_2 is OFF and T_1 is ON, connecting the output to the input and B = A = V(0).

* If C = 0, No transmission is possible.
* **Noise Margin :** Noise margin of CMOS logic IC's is higher than that of TTL.
* **Unconnected Input :** Unused input must be connected to either the supply voltage terminal or one of the used input provided that the fan-out of the signal source is not exceeded.

LOGIC FAMILIES COMPARISON

Logic	RTL	DTL	HTL	TTL	ECL	MOS	CMOS
Gate	N1	N2	N2	N2	N1/N2	N2	N1/N2
Fan-out	5	8	10	10	25	20	50
Power loss mW	12	8	50	12	40	0.2	0.01
Noise	N	G	E	VG	G	N	VG
Propga-tion nsec	12	30	90	12	4	300	70

* N → Normal
* G → Good
* E → Excellent
* N2 → NAND
* S → Satisfactory
* VG → Very good
* N1 → NOR
* N3 → OR