Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S8 (R,S) Exam April 2025 (2019 Scheme)

Course Code: ECT448

Course Name: LOW POWER VLSI

Max. Marks: 100 **Duration: 3 Hours**

PART A

Answer all questions, each carries 3 marks. Marks

1	Explain the hot electron effect with neat diagrams.	(3)
2	Discuss the design issues in deep submicron transistors.	(3)
3	Derive the expression for switching power dissipation.	(3)
4	List various sources of leakage power dissipation.	(3)
5	List out techniques used for power reduction using supply voltage scaling.	(3)
6	Discuss about variable threshold CMOS for leakage power reduction.	(3)
7	List the advantages & disadvantages of clocked circuits.	(3)
8	Explain the concepts of ratioed logic.	(3)
9	Explain the difference between adiabatic charging & Conventional charging.	(3)
10	Draw the circuit diagram of adiabatic amplifier.	(3)

PART B

Answer any one full question from each module, each carries 14 marks.

Module I

11	Explain the MIS structure with neat diagrams when it is i) Unbiased ii) accumulation iii) depletion iv) strong inversion	(14)

OR

12	Explain the following short channel effects with neat diagrams i)Drain induced barrier lowering (DIBL) ii) Impact ionization iii) Surface scattering iv) Punch through & discuss the methods to reduce short channel effects.	(14)

Module II

13	Derive the expression for short circuit power dissipation for a CMOS inverter & discuss short current dependency with input and output load.	(14)

OR

14	a)	Explain the leakage current mechanisms in short channel transistors.	(8)

b) Explain the formation of glitches in circuits & discuss methods used for eliminating the glitches. (6)

Module III

15 a) Describe how transistor stacking is used to reduce leakage current. (6)

b) Explain the term gating. Discuss how clock gating used to reduce power dissipation. (8)

OR

16 Explain dynamic & leakage power reduction using transistor sizing. (14)

Module IV

17 a) Implement X-OR gate using NMOS & Pseudo NMOS logic. (7)

b) Explain the working of differential current switch logic. (7)

OR

18 a) Implement NAND/ AND using DCVS logic & Explain its working with help of a truth table. (8)

b) Explain the working of a dynamic logic circuit. (6)

Module V

19 a) Explain the working of Adiabatic logic gate & list out the steps to convert conventional CMOS logic gate to an adiabatic gate. (8)

b) Describe the importance of pulsed power supply in adiabatic logic. (6)

OR

20 a) Explain two stage adiabatic buffer & calculate the total energy dissipation in the system. (8)

b) Explain about reversible logic gate structures. (6)

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