Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S8 (R,S) Exam April 2025 (2019 Scheme)

Course Code: ECT466

Course Name: ANALOG CMOS DESIGN

Max. Marks: 100 **Duration: 3 Hours**

PART A

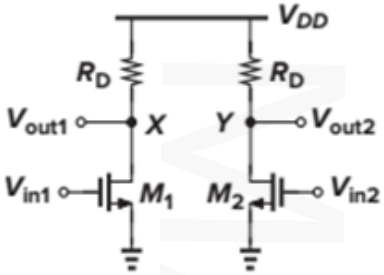
Answer all questions, each carries 3 marks. Marks

1 Comment on sub threshold conduction in MOSFETs. (3)

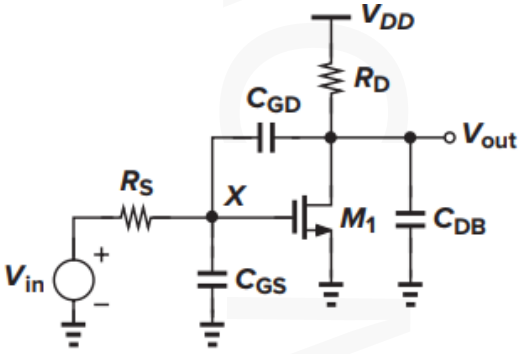
2 Draw the circuit for CS amplifier with current source load and diode connected load. (3)

3 Draw the transfer characteristics of differential output versus differential input voltage($\Delta V_{in}=V_{in1}-V_{in2}$) for a resistive loaded differential amplifier. (3)

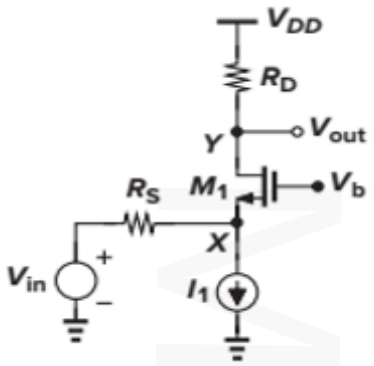
4 What is the main issue with the differential amplifier shown below? (3)



5 Draw the high frequency small signal model of the common source amplifier shown below. (3)

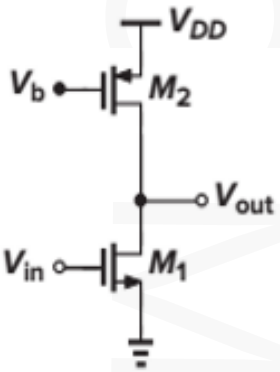


6 Find the input pole of the amplifier using miller approximation (3)



7 Explain flicker noise in a MOSFET and find the noise current due to it in the output circuit. (3)

8 Find the total thermal output noise power per bandwidth of the common source amplifier. (3)



9 Draw and explain the block diagram of a simple PLL (3)

10 What is the advantage of using PFD over a PD in a PLL ? (3)

PART B

Answer any one full question from each module, each carries 14 marks.

Module I

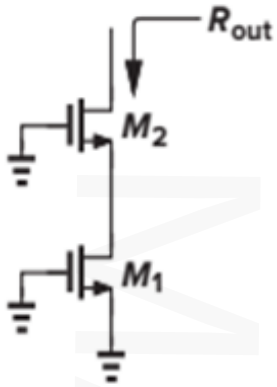
11 a) Comment in detail the large signal operation of the CS amplifier with resistive load. (8)

b) Using small signal analysis find the voltage gain of the above circuit ($\lambda \neq 0$). (6)

OR

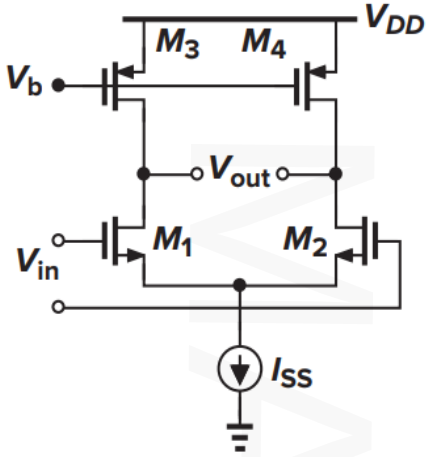
12 a) Derive the expression for voltage gain of a source follower. (7)

b) Find the output resistance (R_{out}) for the circuit diagram shown below. (7)

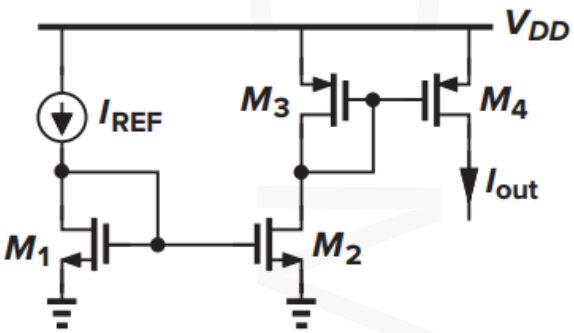


Module II

13 a) Derive the expression of small signal voltage gain of differential amplifier shown. (8)
Assume $g_{m1}=g_{m2}=g_{mN}$ and $g_{m3}=g_{m4}=g_{mP}$.



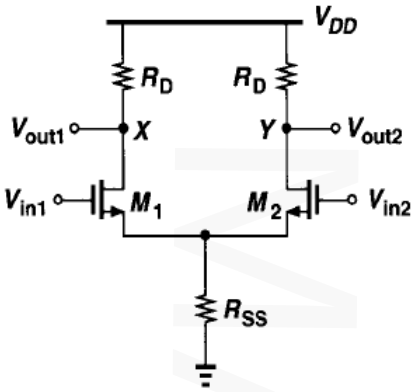
b) Find the drain current of M_4 if all of the transistors are in saturation. I_{REF} = 50µA. (6)
$(W/L)_2=5\ (W/L)_1$ and $(W/L)_4 =4\ (W/L)_3$



OR

14 a) Derive the common mode and differential mode gain for the circuit shown below. (10)

.



b) Comment on the advantages of cascode current mirror over simple current mirror circuits. (4)

Module III

15 a) Draw the high frequency equivalent circuit of source follower and find the voltage transfer function. (14)

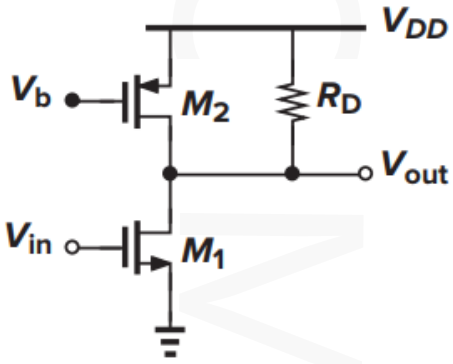
OR

16 a) Explain Miller theorem. (4)

b) Using approximate high frequency model find the poles in a Common Source amplifier. (10)

Module IV

17 a) Calculate the output noise power per unit bandwidth and input-referred 1/f and thermal noise voltage of the CS stage depicted below, assuming M_1 and M_2 are in saturation (λ=0). Trans conductance of MOSFETs are g_{m1}, g_{m2} and dimensions of MOSFETs are $(W/L)_1$ and $(W/L)_2$ (14)



OR

18 a) For an NMOS current source, calculate the total thermal and 1/f noise in the drain (8)

current for a band from 1KHz to 1MHz .

b) Explain the noise analysis procedure to find the total noise at the output due to various noise sources in a circuit. (6)

Module V

19 a) Derive the open loop and closed loop transfer function of a type 1 PLL. (8)

b) How is skew reduction possible using PLL? (6)

OR

20 a) With the help of diagrams, explain the working of a charge-pump (type-2) PLL. Derive expression for the transfer function. (14)

****