ENTRI

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination June 2022 (2019 Scheme)

Course Code: ECT202

Course Name: ANALOG CIRCUITS

Max. Marks: 100 | Duration: 3 Hours (p. 1)

PART A

(Answer all questions; each question carries 3 marks) **(p. 1)**

1. **Draw the circuit of an RC integrator. Give the conditions for an RC circuit to act as integrator. (p. 1)**
2. **Define Stability factor. Derive the expression for stability factor 'S'. (p. 1)**
3. **Differentiate between dc and ac load lines. (p. 1)**
4. **What is the significance of Miller effect on high frequency amplifiers? (p. 1)**
5. **Given** $K = 0.4mA/V^2$ **and** $I_{D(ON)} = 3.5mA$ **with** $V_{GS(ON)} = 4V.$**. Determine the value of** V_{TH} **(p. 1)**
6. **What are the effects of cascading in gain and bandwidth of an amplifier? (p. 1)**
7. **Differentiate positive feedback and negative feedback. (p. 1)**
8. **Draw the block diagrams of current series and current shunt feedback. (p. 1)**
9. **Illustrate the principle of output current boosting circuit in a voltage regulator? (p. 1)**
10. **What do you mean by crossover distortion? How can it be eliminated? (p. 1)**

PART B

(Answer one full question from each module, each question carries 14 marks) **(p. 1)**

Module - 1

11. a) Given an input wave, $V_{in} = 10\sin\omega t$. Setup and explain a clamper that clamps the wave to 22.3V at the positive peak, assuming a voltage drop of 0.7 V across the diode. Draw the output waveform and transfer characteristics also. (8 marks) (p. 1)

b) Design a fixed bias circuit for a CE amplifier such that operating point is $V_{CE} = 8V$ and $I_C = 2mA$. Given, a fixed 15V d.c. supply and a silicon transistor with $\beta = 100$. Take base-emitter voltage $V_{BE} = 0.6V$ and neglect R_E. (6 marks) (p. 1)

OR

12. a) With necessary diagrams, explain any two biasing methods of BJT. (8 marks) (p. 1)

b) Set up and explain a slicer circuit that clips an input sine wave at +2V and +4V. Draw the transfer characteristics. (6 marks) (p. 1)

Module - 2

13. a) Analyse the high frequency response of an amplifier in CE configuration using hybrid π model. (8 marks) (p. 2)

b) Draw and explain the frequency response of RC coupled amplifier. (6 marks) (p. 2)

OR

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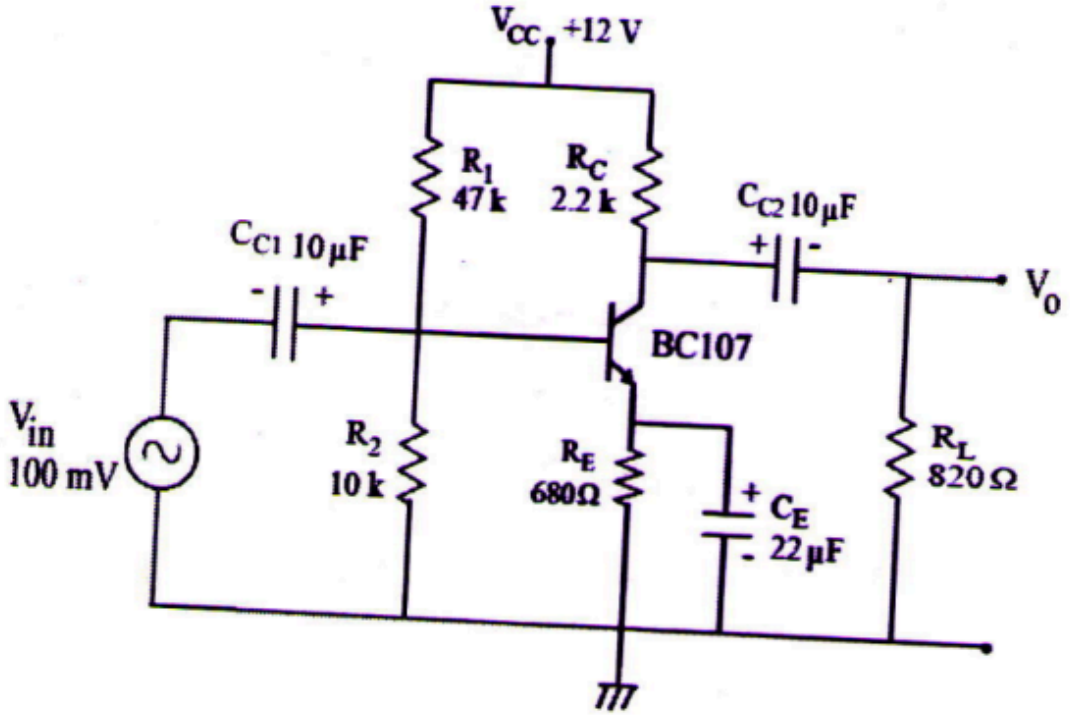
14. Using hybrid π model, calculate the small signal voltage gain, input impedance and output impedance of the given circuit. Given, $V_{BE} = 0.7V, V_A = 80V, I_C = 2mA$ and β = 100. (Neglecting r_o) (14 marks) (p. 2)



Module - 3

15. a) Draw the CS stage with diode connected load and deduce the expression for voltage gain of the amplifier. (8 marks) (p. 2)

b) Calculate the drain current and drain-to-source voltage of a common source circuit with an n-channel enhancement mode MOSFET. Find the power dissipated in the transistor.

$$R_1 = 22K\Omega, R_2 = 10K\Omega, R_D = 6.8K\Omega, V_{DD} = 8V, V_T = 1V, K_n = 0.1mA/V^2$$

(6 marks) (p. 2)

OR

16. a) Draw the circuit of a common source amplifier using MOSFET. Derive the expressions for voltage gain, input resistance

and output resistance from small signal equivalent circuit. (8 marks) (p. 3)

b) Briefly explain a Cascode amplifier. (6 marks) (p. 3)

Module - 4

17. With neat circuit diagram, explain the discrete BJT circuit in voltage-series feedback and derive the expression for voltage gain, input impedance and output impedance. (14 marks) (p. 3)

OR

18. a) Design Wein-bridge oscillator using BJT to generate 1KHz sine wave. (9 marks) (p. 3)

b) With neat circuit diagram, explain the working of Hartley oscillator. (5 marks) (p. 3)

Module - 5

19. What are the factors affecting the variation in output voltage of voltage regulator? With a circuit diagram, explain how load and line regulations are achieved in a shunt voltage regulator. (14 marks) (p. 3)

OR

20. Explain the working of Class B push-pull power amplifier with a neat circuit diagram and output waveforms. Derive the expression for collector efficiency. (14 marks) (p. 3)