APJ Abdul Kalam Technological University Dec 2021

Logic Circuit Design (ECT203) exam paper:

PART A

Answer all questions. Each question carries 3 marks.

1. Convert $(231.45)_8$ to equivalent decimal and binary (p. 1).
2. Give a brief description of keywords in Verilog (p. 1).
3. Reduce the expression $F = \overline{AB + \overline{A} + AB}$ using De-Morgan's theorem (p. 1).
4. Write a Verilog code for implementing a NOR gate (p. 1).
5. Explain the working of a multiplexer (p. 1).
6. Write a Verilog code for half subtractor (p. 1).
7. Convert a JK flipflop to T flipflop (p. 1).
8. Write a Verilog code for implementing D flipflop (p. 1).
9. Define noise-margin (p. 1).
10. Define propagation delay and power dissipation (p. 1).

PART B

Answer any one full question from each module. Each question carries 14 marks.

Module 1

1. (a) Perform the following operations: (p. 1)
   - (i) $(A5C)_{16} + (8E4)_{16}$
   - (ii) $(175.6)_8 - (47.7)_8$

(b) What is Hamming code? The message 1100110 is coded in 7-bit even parity Hamming code which is transmitted through a noisy channel. Decode the message assuming that a single error occurred in the codeword (p. 1).

2. (a) Find 11001 - 10001 using 1's and 2's complement arithmetic (p. 1).
   (b) Explain the operators in Verilog (p. 1).

Module 2

1. (a) Obtain the canonical POS expression of $F(A, B, C) = (A + \overline{B})(B + C)(A + \overline{C})$ (p. 1).
   (b) Simplify the expression $Y = \prod M(0, 1, 4, 5, 6, 8, 9, 12, 13, 14)$ using K-Map and implement the simplified expression using NOR logic (p. 1).
2. For the logical expression $F = \overline{A} + AB + AB\overline{D} + A\overline{B}D + C:$ (p. 2)
   (i) Obtain Canonical SOP expression.
   (ii) Simplify the expression using K-Map.
   (iii) Write Verilog code for the simplified expression.

Module 3

1. (a) Design a full adder circuit (p. 2).
   (b) Write a Verilog code for 1:4 demultiplexer (p. 2).
2. (a) Implement the logic function $f(A, B, C) = \sum m(0, 2, 3, 5)$ using: (p. 2)
   - (i) 8:1 MUX
   - (ii) 4:1 MUX

   (b) Design an octal to binary encoder (p. 2).

Module 4

1. (a) Explain the operation of a JK flip-flop using NAND gates (p. 2).
   (b) Explain the operation of a 4-bit Johnson counter with truth table and waveforms (p. 2).
2. (a) Design a mod-6 synchronous up-counter using JK flip-flop (p. 2).

   (b) Explain a PISO shift register using 

(p. 2).

Module 5

1. (a) Compare TTL & CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay and noise margin (p. 2).
   (b) Draw the circuit and explain the operation of transistor level TTL NAND gate (p. 2).
2. (a) Draw the circuit diagram of a transistor level TTL Inverter and explain the working (p. 2).
   (b) Draw the circuit and explain the operation of transistor level CMOS NAND gate (p. 2).